COLLEGE VISION

To impart value based education in Engineering and Technology to empower young women to meet the societal exigency with a global outlook.

COLLEGE MISSION

- To provide holistic education through innovative teaching-learning practices
- To instill self confidence among rural students by supplementing with co-curricular and extra-curricular activities
- To inculcate the spirit of innovation through training, research and development
- To provide industrial exposure to meet the global challenges
- To create an environment for continual progress through lifelong learning

DEPARTMENT VISION

- To Produce Innovative, Creative, Ethical and Socially responsible Electronics and Communication women engineers to meet the global challenges

DEPARTMENT MISSION

- To create a unique learning environment in Electronics and Communication Engineering to mould a strong engineer with professional ethics
- To provide practical exposure to compete in the global market
- Fostering culture of innovation, research and lifelong learning

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M.E. VLSI DESIGN
Regulation 2023
CHOICE BASED CREDIT SYSTEM

PROGRAMME EDUCATIONAL OBJECTIVES (PEO_S)

PEO I. To acquire a background in Basic science and Mathematics and ability to use these tools in VLSI Design.

PEO II. Teach students to understand the principles involved in the latest software required for designing and critically analyzing electronic systems relevant to industry and society.

PEO III. To attain the qualities of professional leadership to deliver effectively in a multi-disciplinary team and domains

PEO IV. Mould students to be able to communicate efficiently

PEO V. Motivate students to take up socially relevant and challenging projects and propose innovative solution to problems for the benefit of society.

PROGRAM SPECIFIC OUTCOMES (PSOs):

At the end of this program, graduate will be able to:

PSO 1: Comprehend the basic concepts of VLSI Design and apply them in the day to day life to design and execute complete engineering systems.

PSO 2: Design, verify and validate VLSI functional elements for numerous applications including signal processing, communications, computer networks.

PSO 3: Demonstrate the intellectual level with peer engineers and others to work together to arrive at a cost-effective, appropriate solution for various problems.

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PROGRAMME OUTCOMES (POs)

PO 1. Apply knowledge of Mathematics, Science, Engineering fundamentals and an Engineering specialization to the conceptualization of Engineering models.

PO 2. Identify, formulate, research literature and solve complex Electronics and communication engineering problems reaching substantiated conclusions using first principles of Mathematics and Engineering sciences.

PO 3. Design solutions for complex Electronics and Communication Engineering problems and design systems, components or processes that meet specified needs with appropriate consideration for public health and safety, cultural, societal, and environmental considerations.

PO 4. Conduct investigations of complex problems including design of experiments, analysis and interpretation of data, and synthesis of information to provide valid conclusions.

PO 5. Create, select and apply appropriate techniques, resources, and modern Engineering tools, including prediction and modeling, to complex Electronics and Communication Engineering activities, with an understanding of the limitations.

PO 6. Function effectively as an individual, and as a member or leader in diverse teams and in multi - disciplinary settings.

PO 7. Communicate effectively on complex Electronics and Communication Engineering activities with the Engineering community and with society at large, such as being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

PO 8. Demonstrate understanding of the societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to Engineering practice.

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PO 9. Understand and commit to professional ethics and responsibilities and norms of engineering practice.

PO 10. Understand the impact of engineering solutions in a societal context and demonstrate knowledge of and need for sustainable development.

PO 11. Demonstrate a knowledge and understanding of management and business practices, such as risk and change management, and understand their limitations.

PO 12. Recognize the need for, and have the ability to engage in independent and lifelong learning.

MAPPING OF PROGRAMME EDUCATIONAL OBJECTIVES (PEO_S) WITH PROGRAMME OUTCOMES (PO_S)

A broad relation between the programme educational objective and the outcomes is given in the following table

PROGRAMME EDUCATIONAL OBJECTIVES	PROGRAMME OUTCOMES											
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12
PEO 1	✓	✓					✓					
PEO 2			✓	✓	✓							✓
PEO 3				✓		✓						
PEO 4						✓				✓	✓	
PEO 5						✓	✓	✓	✓	✓	✓	✓

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SEM	Course	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO 9	PO10	PO11	PO12
I	Applied Mathematics	✓	✓	✓		✓							
	Analog IC Design	✓	✓	✓		✓							
	VLSI Digital Signal Processing	✓	✓	✓		✓							
	Professional Elective – I												
	Professional Elective – II												
	Audit Course I												
	Analog VLSI System Laboratory	✓	✓			✓			✓	✓	✓		
	Electronic Design Automation Laboratory	✓	✓			✓			✓	✓	✓		
II	Low Power VLSI Design	✓	✓	✓		✓							
	Testing and Verification of VLSI Circuits	✓	✓	✓		✓							
	VLSI for Wireless Communication	✓	✓	✓		✓							
	Professional Elective – III												
	Professional Elective – IV												
	Audit Course II												
	Digital VLSI System Laboratory	✓	✓			✓			✓	✓	✓		
	VLSI Design Verification and Testing Laboratory	✓	✓			✓			✓	✓	✓		
	Mini Project-I	✓	✓			✓			✓	✓	✓		
III	ASIC Design	✓	✓	✓		✓							
	Professional Elective – V												
	Open Elective - I												
	Dissertation Phase -I	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
IV	Dissertation Phase – II	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

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Programme	**M.E.**	Programme Code	**205**	Regulation	**2023**
Department	**VLSI DESIGN / ELECTRONICS AND COMMUNICATION ENGINEERING**			Semester	**I**

CURRICULUM

(Applicable to the students admitted from the academic year 2023-2024 onwards)

Course Code	Course Name	Category	Periods / Week			Credit	Maximum Marks		
			L	T	P	C	CA	ESE	Total
THEORY									
P23MA102	Applied Mathematics	FC	3	0	0	3	40	60	100
P23VD101	Analog IC Design	PCC	3	0	0	3	40	60	100
P23VD102	VLSI Digital Signal Processing	PCC	3	0	0	3	40	60	100
	Professional Elective – I	PEC	3	0	0	3	40	60	100
	Professional Elective – II	PEC	3	0	0	3	40	60	100
	Audit Course-I	AC	2	0	0	0	100	-	100
PRACTICAL									
P23VD103	Analog VLSI System Laboratory	PCC	0	0	4	2	60	40	100
P23VD104	Electronic Design Automation Laboratory	PCC	0	0	4	2	60	40	100
					Total Credits	**19**	**420**	**380**	**800**

PCC – Professional Core Course, PEC – Professional Elective Course, AC- Program Audit Course, FC- Foundational Course, CA - Continuous Assessment, ESE - End Semester Examination

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Programme	**M.E.**	Programme Code	**205**	Regulation	**2023**
Department	**VLSI DESIGN / ELECTRONICS AND COMMUNICATION ENGINEERING**			Semester	**II**

CURRICULUM

(Applicable to the students admitted from the academic year 2023-2024 onwards)

Course Code	Course Name	Category	Periods / Week			Credit	Maximum Marks		
			L	T	P	C	CA	ESE	Total
THEORY									
P23VD205	Low Power VLSI Design	PCC	3	0	0	3	40	60	100
P23VD206	Testing and Verification of VLSI Circuits	PCC	3	0	0	3	40	60	100
P23VD207	VLSI for Wireless Communication	PCC	3	0	0	3	40	60	100
	Professional Elective – III	PEC	3	0	0	3	40	60	100
	Professional Elective – IV	PEC	3	0	0	3	40	60	100
	Audit Course-II	AC	2	0	0	0	100	-	100
PRACTICAL									
P23VD208	Digital VLSI System Laboratory	PCC	0	0	4	2	60	40	100
P23VD209	VLSI Design Verification and Testing Laboratory	PCC	0	0	4	2	60	40	100
P23VD210	Mini Project-I	EEC	0	0	4	2	100	-	100
					Total Credits	**21**	**460**	**440**	**900**

PCC – Professional Core Course, PEC – Professional Elective Course, AC- Program Audit Course,
CA - Continuous Assessment, ESE - End Semester Examination

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Programme	**M.E.**	Programme Code	**205**	Regulation	**2023**
Department	**VLSI DESIGN / ELECTRONICS AND COMMUNICATION ENGINEERING**			Semester	**III**

CURRICULUM

(Applicable to the students admitted from the academic year 2023-2024 onwards)

Course Code	Course Name	Category	Periods / Week			Credit	Maximum Marks		
			L	T	P	C	CA	ESE	Total
THEORY									
P23VD311	ASIC Design	PCC	3	0	0	3	40	60	100
	Professional Elective –V	PEC	3	0	0	3	40	60	100
	Open Elective – I	OEC	3	0	0	3	40	60	100
PRACTICAL									
P23VD312	Dissertation Phase –I	EEC	0	0	16	8	60	40	100
					Total Credits	**17**	**180**	**220**	**400**

PCC – Professional Core Course, PEC – Professional Elective Course, OEC- Open Elective Course,
EEC – Employability Enhancement Course, CA - Continuous Assessment, ESE - End Semester Examination

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Programme	**M.E.**	Programme Code	**205**	Regulation	**2023**
Department	**VLSI DESIGN / ELECTRONICS AND COMMUNICATION ENGINEERING**			Semester	**IV**

CURRICULUM

(Applicable to the students admitted from the academic year 2023-2024 onwards)

Course Code	Course Name	Category	Periods / Week			Credit	Maximum Marks		
			L	T	P	C	CA	ESE	Total
PRACTICAL									
P23VD413	Dissertation Phase – II	EEC	0	0	32	16	60	40	100
					Total Credits	**16**	**60**	**40**	**100**

EEC – Employability Enhancement Course, CA - Continuous Assessment, ESE - End Semester Examination

Cumulative Course Credits -73

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PROFESSIONAL CORE COURSES (PCC)

Course Code	Course Name	Category	Periods / Week			Credit	Maximum Marks		
			L	T	P	C	CA	ESE	Total
P23VD101	Analog IC Design	PCC	3	0	0	3	40	60	100
P23VD102	VLSI Digital Signal Processing	PCC	3	0	0	3	40	60	100
P23VD103	Analog VLSI System Laboratory	PCC	0	0	4	2	60	40	100
P23VD104	Electronic Design Automation Laboratory	PCC	0	0	4	2	60	40	100
P23VD205	Low Power VLSI Design	PCC	3	0	0	3	40	60	100
P23VD206	Testing and Verification of VLSI Circuits	PCC	3	0	0	3	40	60	100
P23VD207	VLSI for Wireless Communication	PCC	3	0	0	3	40	60	100
P23VD208	Digital VLSI System Laboratory	PCC	0	0	4	2	60	40	100
P23VD209	VLSI Design Verification and Testing Laboratory	PCC	0	0	4	2	60	40	100
P23VD311	ASIC Design	PCC	3	0	0	3	40	60	100

ENHANCED EMPLOYABILITY COURSES (EEC)

Course Code	Course Name	Category	Periods / Week			Credit	Maximum Marks		
			L	T	P	C	CA	ESE	Total
P23VD210	Mini Project-I	EEC	0	0	4	2	60	40	100
P23VD312	Dissertation Phase -I	EEC	0	0	16	8	60	40	100
P23VD413	Dissertation Phase – II	EEC	0	0	32	16	60	40	100

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FOUNDATION COURSE (FC)

Course Code	Course Name	Category	Periods / Week			Credit	Maximum Marks		
			L	T	P	C	CA	ESE	Total
P23MA102	Applied Mathematics	FC	3	0	0	3	40	60	100

PROFESSIONAL ELECTIVE - I

Course code	Course Name	Category	L	T	P	C	CA	ESE	Total
P23VDE01	Embedded System Design	PEC	3	0	0	3	40	60	100
P23VDE02	Physics of MOS Transistors	PEC	3	0	0	3	40	60	100
P23VDE03	Foundations of VLSI CAD	PEC	3	0	0	3	40	60	100
P23VDE04	HDL with System Modeling	PEC	3	0	0	3	40	60	100

PROFESSIONAL ELECTIVE - II

Course code	Course Name	Category	L	T	P	C	CA	ESE	Total
P23VDE05	Introduction to MEMS	PEC	3	0	0	3	40	60	100
P23VDE06	Multimedia Compression Techniques	PEC	3	0	0	3	40	60	100
P23VDE07	Semiconductor Memory Design	PEC	3	0	0	3	40	60	100
P23VDE08	System on Chip Design	PEC	3	0	0	3	40	60	100

PROFESSIONAL ELECTIVE – III

Course code	Course Name	Category	L	T	P	C	CA	ESE	Total
P23VDE09	Hardware Design Verification Techniques	PEC	3	0	0	3	40	60	100
P23VDE10	RF Microelectronics Chip Design	PEC	3	0	0	3	40	60	100
P23VDE11	Mixed Signal VLSI Design	PEC	3	0	0	3	40	60	100
P23VDE12	Nano Electronics	PEC	3	0	0	3	40	60	100

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PROFESSIONAL ELECTIVE - IV

Course code	Course Name	Category	L	T	P	C	CA	ESE	Total
P23VDE13	Processors and Embedded Controllers	PEC	3	0	0	3	40	60	100
P23VDE14	Digital System Design With FPGA	PEC	3	0	0	3	40	60	100
P23VDE15	Speech and Audio Signal Processing	PEC	3	0	0	3	40	60	100
P23VDE16	Internet of Things And Applications	PEC	3	0	0	3	40	60	100

PROFESSIONAL ELECTIVE - V

Course code	Course Name	Category	L	T	P	C	CA	ESE	Total
P23VDE17	Soft Computing	PEC	3	0	0	3	40	60	100
P23VDE18	Networks on Chip	PEC	3	0	0	3	40	60	100
P23VDE19	ARM processor and architecture	PEC	3	0	0	3	40	60	100
P23VDE20	Wireless Adhoc and Sensor Networks	PEC	3	0	0	3	40	60	100

OPEN ELECTIVE OFFERED TO OTHER DEPARTMENTS

Course code	Course Name	Category	L	T	P	C	CA	ESE	Total
P23VDOE1	Micro sensors and MEMS	OEC	3	0	0	3	40	60	100
P23VDOE2	Basics of VLSI	OEC	3	0	0	3	40	60	100
P23VDOE3	Communication Busses and Interfaces	OEC	3	0	0	3	40	60	100

OPEN ELECTIVE (EEE)

Course code	Course Name	Category	L	T	P	C	CA	ESE	Total
P23PSOE1	Industrial Safety	OEC	3	0	0	3	40	60	100
P23PSOE2	Energy storage Technologies	OEC	3	0	0	3	40	60	100
P23PSOE3	Energy Management and Auditing	OEC	3	0	0	3	40	60	100
P23PSOE4	Electrical Circuit design for Hazardous in Industries	OEC	3	0	0	3	40	60	100

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OPEN ELECTIVE (CSE)

Course code	Course Name	Category	L	T	P	C	CA	ESE	Total
P23CSOE1	Business Analytics	OEC	3	0	0	3	40	60	100
P23CSOE2	Machine Learning Techniques	OEC	3	0	0	3	40	60	100
P23CSOE3	Web Engineering	OEC	3	0	0	3	40	60	100
P23CSOE4	Cost Management of Engineering Projects	OEC	3	0	0	3	40	60	100
P23CSOE5	Internet of Things	OEC	3	0	0	3	40	60	100
P23CSOE6	Data Science and Analytics	OEC	3	0	0	3	40	60	100

OPEN ELECTIVE (IT)

Course code	Course Name	Category	L	T	P	C	CA	ESE	Total
P23ITOE1	Cloud Computing Principles	OEC	3	0	0	3	40	60	100
P23ITOE2	Research Publication Ethics	OEC	3	0	0	3	40	60	100
P23ITOE3	Game Development	OEC	3	0	0	3	40	60	100
P23ITOE4	IoT for Smart System	OEC	3	0	0	3	40	60	100
P23ITOE5	Robotics	OEC	3	0	0	3	40	60	100

OPEN ELECTIVE (BioTech)

Course code	Course Name	Category	L	T	P	C	CA	ESE	Total
P23BTOE1	Bioethics and Biosafety	OEC	3	0	0	3	40	60	100
P23BTOE2	Renewable Bioenergy	OEC	3	0	0	3	40	60	100
P23BTOE3	Waste Management	OEC	3	0	0	3	40	60	100

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AUDIT COURSES (AC)

Course Code	Course Name	Category	Periods / Week			Credit	Maximum Marks		
			L	T	P	C	CA	ESE	Total
AUDIT COURSE-I									
P23AC001	Research Process and Methodologies	AC	2	0	0	0	100	0	100
P23AC002	Pedagogy Studies	AC	2	0	0	0	100	0	100
P23AC003	Disaster Management	AC	2	0	0	0	100	0	100
P23AC004	Value Education	AC	2	0	0	0	100	0	100
P23AC005	Constitution of India	AC	2	0	0	0	100	0	100
AUDIT COURSE-II									
P23AC006	English for Research Paper Writing	AC	2	0	0	0	100	0	100
P23AC007	Personality Development through Life Enlightenment	AC	2	0	0	0	100	0	100
P23AC008	Universal Human Values	AC	2	0	0	0	100	0	100
P23AC009	Online Course	AC	2	0	0	0	100	0	100

S.No.	Course Components	Credits per semester				Total number of credits for each component
		I	II	III	IV	
1	Foundational Course (FC)	3	-	-	-	3
2	Programme Core Courses (PCC)	10	13	3	-	26
3	Professional Elective Course (PEC)	6	6	3	-	15
4	Open Electives (OE)	-	-	3	-	3
5	Employability Enhancing Courses (EEC)	-	2	8	16	26
6	Programme Audit Course (AC)	-	-	-	-	-
Total Credits		20	21	17	16	73

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Programme	**M.E.**	Programme Code			**205**	Regulation	**2023**	
Department	**VLSI/ / ELECTRONICS AND COMMUNICATION ENGINEERING**					Semester	**I**	
Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P23MA102	**Applied Mathematics**	3	0	0	3	**40**	**60**	**100**

Course Objective

The main objective of the course is to

- Acquaint the knowledge of testing of hypothesis for small and large samples which plays an important role in real life problems.
- Understand the concepts of ANOVA.
- Identify and demonstrate suitable sampling and data collection process.
- Identify the formulation and graphical solution of linear programming problem.
- Potentially understand forward and backward recursion.

Course Outcome

At the end of the course, the student should be able to	Knowledge Level
CO1: Apply the concept of testing of hypothesis for small and large samples in real life problems.	K4
CO2: Apply the basic concepts of classifications of design of experiments in the field of agriculture.	K5
CO3: Apply appropriate modern technology to explore probability/statistical concepts.	K3
CO4: Incorporate Transportation and Assignment problems.	K3
CO5: Recognize Dynamic programming applications using Loading method.	K5

Pre-requisites

CO / PO Mapping (3/2/1 indicates strength of correlation) 3-Strong, 2 – Medium, 1 - Weak													**CO/PSO Mapping**		
COs	Programme Outcomes (POs)												PSOs		
	PO 1	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO 10**	**PO 11**	**PO 12**	**PSO 1**	**PSO 2**	**PSO 3**
CO 1	3	2	1		1								2		
CO 2	3		1		1								2		
CO 3	3	2		1									2		
CO 4	3	2	1	1	1								2		
CO 5	3	2	1	1									2		

Course Assessment Methods

Direct
1. Continuous Assessment Test I, II & III 2. Assignment and Seminar. 3. End-Semester examinations
Indirect
1. Course - end survey

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Content of the syllabus			
Unit – I	**TESTING OF HYPOTHESIS**	Periods	**9**
Sampling distributions - Estimation of parameters - Statistical hypothesis - Large sample tests based on Normal distribution for single mean and difference of means -Tests based on t, Chi-square and F distributions for mean, variance and proportion - Contingency table (test for independent) - Goodness of fit.			
Unit - II	**DESIGN OF EXPERIMENTS**	Periods	**9**
One way and two way classifications - Completely randomized design – Randomized block design – Latin square design – 2^2 factorial design.			
Unit – III	**ESTIMATION THEORY**	Periods	**9**
Sampling distributions, point estimation, unbiasedness, consistency, maximum likelihood estimation, Confidence intervals for parameter in one sample from normal population.			
Unit - III	**LINEAR PROGRAMMING**	Periods	**9**
Formulation-Graphical solution-Simplex Method -Transportation and Assignment problems			
Unit - V	**DYNAMIC PROGRAMMING**	Periods	**9**
Dynamic Programming-principle of optimality-forward and backward recursion-DP Applications (Cargo loading method)-Problems of dimensionality.			
		Total Periods	**45**

Text Books	
1.	Douglas.C; Montgomery, 'Applied Statistics and Probability for Engineers', 6th Edition, Wiley Students Edition, Wiley, 2017.
2.	Hamdy A. Taha., 'Operations Research: An Introduction', 9th Edition, Pearson New Delhi, 2014.
References	
1.	Richard. A. Johnson , Irwin Miller,' Probability And Statistics For Engineers', 8th Edition, Pearson Education, Delhi, 2020.
2.	Kalyanmoy Deb., 'Optimization For Engineering Design', Phi, 2004.
3.	Kanti B. Datta., 'Mathematical Methods Of Science And Engineering', Cengage Learning, 2013.
4.	Ronald E.Walpole & Raymond H.Myers 'Probability And Statistics For Engineers And Scitintists', Pearson Education,Delhi, 9th Edition, 2014.
5.	Kothari.C.R., 'An Introduction To Operational Research' 3rd Edition, VIKAS, New Delhi, 2010.
E-Resources	
1.	*https://online.stanford.edu* ›
2.	www.learnerstv.com/Free-engineering-Video-lectures
3.	www.nptel.ac.in

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Programme	**M.E.**	Programme Code		**205**	Regulation		**2023**	
Department	**VLSI DESIGN / ELECTRONICS AND COMMUNICATION ENGINEERING**				Semester		**I**	
Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P23VD101	**Analog IC Design**	3	0	0	3	40	60	**100**

Course Objective	The main objective of the course is • To illustrate the MOS Devices Modeling techniques and IC packaging types • To comprehend the concept of Current Source, sink and Reference Circuits. • To design CMOS Amplifiers • To learn about Data converters and architectures • To realize the different types of Comparators	
Course Outcome	At the end of the course, the student should be able to	Knowledge Level
	CO1: Model various components in CMOS process to estimate their performance in circuits	K3
	CO2: Analyze and design current source circuits	K4
	CO3: Design of various CMOS Amplifiers	K4
	CO4: Construct the different types of converters	K3
	CO5: Summarize the Characteristics of Comparator circuits	K2
Pre-requisites	EDC,LIC,EC-I & II	

CO / PO Mapping (3/2/1 indicates strength of correlation) 3-Strong, 2 – Medium, 1 - Weak													**CO/PSO Mapping**		
COs	Programme Outcomes (POs)												PSOs		
	PO 1	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO 10**	**PO 11**	**PO 12**	**PSO 1**	**PSO 2**	**PSO 3**
CO 1	3	3	3	2		1						1	3	2	
CO 2	3	3	3	2		1						1	3	2	
CO 3	3	3	2	2		1						1	3	2	
CO 4	3	3	3	2		1						1	3	2	
CO 5	3	3	3	2		1						1	3	2	

Course Assessment Methods

Direct
1. Continuous Assessment Test I, II & III 2. Assignment, Seminar and Quiz 3. End-Semester examinations
Indirect
1. Course - end survey

Content of the syllabus

Unit – I	**MOS Devices Modeling and IC Packaging**	Periods	**9**

The MOS Transistor, Passive Components- Capacitor & Resistor, Integrated circuit Layout, CMOS Device

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Modeling - Other Model Parameters, Small-Signal Model for the MOS Transistor, Computer Simulation Models, Sub-threshold MOS Model. IC Packaging: Types and Modeling-Electrical Package Modeling-Thermal Modeling- Stress Modeling-Package Simulation- Flip-Chip Package.			
Unit – II	**CURRENT SOURCE-SINK AND REFERNCES**	Periods	**9**
The Current Mirror: The Cascode Connection-Sensitivity Analysis-Temperature Analysis-Transient Response-Layout of the Simple Current Mirror-matching in MOSFET Mirrors-References: Voltage Dividers- Current Source Self Biasing: Threshold Voltage Referenced Self-Biasing- Band gap Voltage References-Beta Multiplier Referenced Self Biasing.			
Unit – III	**AMPLIFIERS**	Periods	**9**
Amplifiers: Gate-Drain Connected Loads-Current Source Loads-Noise and Distortion in Amplifiers-Feedback Amplifiers: Properties of Negative Feedback on Amplifier Design-Recognizing Feedback Topologies- Voltage Amplifier- Transimpedance Amplifier –Transconductance Amplifier – Current Amplifier-Output Amplifier-Cascode Amplifiers-Source Follower-Voltage Level Shifter-CMOS Operational Amplifier- Differential Amplifier.			
Unit – IV	**DATA CONVERTERS AND ARCHITECTURES**	Periods	**9**
Analog Versus Discrete Time Signals- S/H Characteristics- Mixed Signal Layout Issues-DAC Specifications and Architectures: Digital Input Code- Resistor String-R-2R Ladder networks-Current Steering-Charge Scaling DACs-Cyclic DAC- Pipeline DAC- ADC Specifications and Architectures: Flash-Two-Step Flash ADC-Pipeline ADC-Integrating ADC-Successive Approximation ADC-Oversampling ADC.			
Unit – V	**COMPARATORS**	Periods	**9**
Characterization of Comparator, Two-Stage, Open-Loop Comparators, Other Open-Loop Comparators, Improving the Performance of Open-Loop Comparators, Discrete-Time Comparators.			
		Total Periods	**45**

References

1.	CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Third Edition/Indian Edition, 2013.
2.	R. Jacob Baker, Harry W. Li, David E. Boyce, —CMOS Circuit Design, Layout and Simulation‖, IEEE Press Series on Microelectronics Systems Stuart K. Tewksbuy, Series Edition,1998.
3.	Debaprasad Das, —VLSI Design, Oxford University Press, 2nd edition ,2015

E-Resources

E1	https://nptel.ac.in/courses/117101105/Prof. A.N. Chandorkar
E2	https://www.btechguru.com/courses--nptel--cmos-analog-vlsi-design-video-lecture.html

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Programme	**M.E.**	Programme Code	**205**	Regulation	**2023**		
Department	**VLSI DESIGN / ELECTRONICS AND COMMUNICATION ENGINEERING**			Semester	**I**		

Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P23VD102	**VLSI Digital Signal Processing**	3	0	0	3	40	60	100

Course Objective

The main objective of the course is

- To study the DSP Systems, Pipelining and parallel processing of FIR Filters.
- To understand the concept of Retiming, Algorithmic strength reduction.
- To explore the Fast Convolution, Pipelining and Parallel Processing of IIR Filters.
- To understand Scaling, Round-Off Noise, Bit-Level Arithmetic Architectures and Numerical Strength Reduction.
- To understand Synchronous, Wave and Asynchronous Pipelining.

Course Outcome	At the end of the course, the student should be able to	Knowledge Level
	CO1: Acquire the knowledge of round off noise computation.	K2
	CO2: Acquire the knowledge of Algorithmic Strength reduction.	K2
	CO3: Apply convolution and IIR Filters concept in signal processing applications.	K3
	CO4: Design Bit level and redundant arithmetic Architectures.	K5
	CO5: Acquire the knowledge of numerical strength reduction.	K3

Pre-requisites Digital Signal Processing

CO / PO Mapping (3/2/1 indicates strength of correlation) 3-Strong, 2 – Medium, 1 - Weak												**CO/PSO Mapping**		
COs	Programme Outcomes (POs)											PSOs		
	PO 1	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO 10**	**PO 11**	**PO 12**	**PSO 1**	**PSO 2**	**PSO 3**
CO 1	3	3	3	2									3	2	1
CO 2	3	3	3	2									3	2	1
CO 3	3	3	3	2									3	2	1
CO 4	3	3	3	2									3	2	1
CO 5	3	3	3	2									3	2	1

Course Assessment Methods

Direct
1. Continuous Assessment Test I, II & III 2. Assignment and Seminar 3. End-Semester examinations
Indirect
1. Course - end survey

Content of the syllabus

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Unit – I	**INTRODUCTION TO DSP SYSTEMS, PIPELINING AND PARALLEL PROCESSING OF FIR FILTERS**	Periods	**9**
Introduction To DSP Systems -Typical DSP algorithms; Iteration Bound – data flow graph representations, loop bound and iteration bound, Longest path Matrix algorithm; Pipelining and parallel processing – Pipelining of FIR digital filters, parallel processing, pipelining and parallel processing for low power.			
Unit – II	**RETIMING, ALGORITHMIC STRENGTH REDUCTION**	Periods	**9**
Retiming - definitions and properties; Unfolding – an algorithm for Unfolding, properties of unfolding, sample period reduction and parallel processing application; Algorithmic strength reduction in filters and transforms – 2-parallel FIR filter, 2-parallel fast FIR filter, DCT algorithm architecture transformation, parallel architectures for rank-order filters, Odd- Even Merge- Sort architecture, parallel rank-order filters.			
Unit – III	**FAST CONVOLUTION, PIPELINING AND PARALLEL PROCESSING OF IIR FILTERS**	Periods	**9**
Fast convolution – Cook-Toom algorithm, modified Cook-Toom algorithm, Pipelined and parallel recursive filters – Look-Ahead pipelining in first-order IIR filters, Look-Ahead pipelining with power-of-2 decomposition, Clustered look-ahead pipelining, Parallel processing of IIR filters, combined pipelining and parallel processing of IIR filters.			
Unit – IV	**SCALING, ROUND-OFF NOISE, BIT-LEVEL ARITHMETIC ARCHITECTURES**	Periods	**9**
Scaling and round-off noise – scaling operation, round-off noise, state variable description of digital filters, scaling and round-off noise computation, round-off noise in pipelined IIR filters, Bit-level arithmetic architectures – parallel multipliers with sign extension, parallel carry-ripple and carry-save multipliers, Design of Lyon's bit-serial multipliers using Horner's rule, bit-serial FIR filter, CSD representation, CSD multiplicationusingHorner'sruleforprecisionimprovement,DistributedArithmeticfundamentalsandFIR filters.			
Unit – V	**NUMERICAL STRENGTH REDUCTION, SYNCHRONOUS, WAVE AND ASYNCHRONOUS PIPELINING**	Periods	**9**
Numerical strength reduction – sub expression elimination, multiple constant multiplication, iterative matching, synchronous pipelining and clocking styles, clock skew in edge-triggered single phase clocking, Two-phase clocking, wave pipelining. Asynchronous pipelining bundled data versus dual rail protocol.			
		Total Periods	**45**

References	
1.	K.K.Parhi, "VLSI Digital Signal Processing Systems", John-Wiley, 2007
2.	U. Meyer -Baese, "Digital Signal Processing with FPGAs", Springer, 2014

E-Resources	
E1	https://d1.amobbs.com/bbs_upload782111/files_18/ourdev_480582.pdf
E2	https://books.google.co.in/books/about/VLSI_DIGITAL_SIGNAL_PROCESSING_SYSTEMS_D.html?id=APFRHFkMqG8C
E3	https://onlinecourses.nptel.ac.in/noc20_ee44/preview
E4	http://www.ece.umn.edu/users/parhi/SLIDES/chap2.pdf

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Programme	M.E.	Programme Code	205	Regulation	2023
Department	VLSI DESIGN / ELECTRONICS AND COMMUNICATION ENGINEERING			Semester	I

Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P23VD103	**Analog VLSI System Laboratory**	0	0	4	2	60	40	100

Course Objective

The main objective of the course is
- To design a sequential circuit using HDL
- To implement ALU and MAC in FPGA
- To simulate circuits using Xilinx/EDA Tool
- To simulate circuits using MATLAB/EDA Tool
- To implement DSP Algorithms

Course Outcome

At the end of the course, the student should be able to	Knowledge Level
CO1: Design a sequential circuit using HDL	K4
CO2 : Implement ALU and MAC in FPGA	K4
CO3 : Analyze Circuit simulation using Xilinx/EDA Tool	K3
CO4 : Analyze Circuit simulation using MATLAB/EDA Tool	K3
CO5 : Implement DSP Algorithms	K2

Pre-requisites -

CO / PO Mapping (3/2/1 indicates strength of correlation) 3-Strong, 2 – Medium, 1 - Weak													CO/PSO Mapping		
Cos	Programme Outcomes (POs)												PSOs		
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2	PSO 3
CO 1	3				3								3	2	
CO 2	3				3								3	2	
CO 3	3				3								3	2	
CO 4	3				3								3	2	
CO 5	3				3								3	2	

Course Assessment Methods

Direct
1. Pre lab and Post lab Test.
2. End-Semester examinations
Indirect
1. Course – end survey

Content of the syllabus

S.No	Suggested List of Experiments:	CO Mapping
1	Modeling of Sequential Digital system using VHDL	CO1
2	Modeling of Sequential Digital system using VERILOG	CO1

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3	Design and Implementation of ALU using FPGA	CO2
4	Simulation of NMOS and CMOS circuits using Xilinx/EDA Tool	CO3
5	Modeling of MOSFET using C	CO4
6	Implementation of FFT, Digital Filters in DSP Processor	CO4
7	Implementation of DSP algorithms using software package	CO5
8	Implementation of MAC Unit using FPGA	CO2
	Total Periods	**45**

References	
1.	An Introduction to VHDL overview, Dinesh Sharma, 2008. vhdl-overview.pdf (iitb.ac.in)
2.	U. Meyer -Baese, —Digital Signal Processing with FPGAsll, Springer, 2014
E-Resources	
E1	Synthesis of Digital Systems - Course (nptel.ac.in)
E2	Matlab Programming for Numerical Computation - Course (nptel.ac.in)

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Programme	**M.E.**	Programme Code	**205**	Regulation	**2023**		
Department	**VLSI DESIGN/ ELECTRONICSAND COMMUNICATION ENGINEERING**		Semester		**I**		

Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P23VD104	**Electronic Design Automation lab**	0	0	4	2	60	40	100

Course Objective	The main objective of the course is • To introduce HDL modeling and simulation at RTL abstraction of combinational and sequential subsystems. • To provide understanding of writing proper test benches. • To provide exposure to different HDL modeling styles and their applications. • To introduce background in assessing the impact of coding styles on synthesis.	
Course Outcome	At the end of the course, the student should be able to	Knowledge Level
	CO1 : Understand various modeling styles.	K2
	CO2 : Apply modeling styles for realizing digital subsystems.	K3
	CO3 : Verify and analyze HDL models by writing appropriate test benches.	K4
	CO4 : Evaluate the impact of coding styles on synthesis.	K5
	CO5 : Develop RTL architectures for simple digital systems.	K2
Pre-requisites	-	

CO / PO Mapping (3/2/1 indicates strength of correlation) 3-Strong, 2 – Medium, 1 - Weak													**CO/PSO Mapping**		
Cos	Programme Outcomes (POs)												PSOs		
	PO 1	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO 10**	**PO 11**	**PO 12**	**PSO 1**	**PSO 2**	**PSO 3**
CO 1	3	2	2										3	2	
CO 2	3	2	3										3	2	
CO 3	3	2	2										3	2	
CO 4	3	2	3										3	2	
CO 5	3	2	2										3	2	

Course Assessment Methods

Direct
1. Pre lab and Post lab Test. 2. End-Semester examinations
Indirect
1. Course - end survey

Content of the syllabus

S.No	**Suggested List of Experiments:**	**CO Mapping**

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1	Introduction to HDL Simulation Flow	CO1
2	Structural, Behavioral and Dataflow Modeling in Verilog	CO1
3	Arithmetic Units: Adders and Subtractors	CO2
4	Behavioral Modeling and Verification of Flip-Flops, Registers and Counters	CO3
5	Behavioral Modeling, Synthesis and FPGA implementation of Flip-flops, Registers and Counters	CO3
6	Behavioral Modeling and Verification of Finite State Machines	CO3
7	Dataflow Modeling and Verification of Multiplexers and Demultiplexers	CO3
8	Memory Subsystem Design	CO4
9	Transistor Level implementation of CMOS circuits- Basic Logic Gates: Inverter, NAND and NOR.	CO4
10	Transistor Level implementation of 4:1 Multiplexer	CO4
11	Mini project: Development of HDL code for MAC unit and realization of FIR Filter	CO5
	Total Periods	**45**

References

1.	Stephen Brown and Zvonko Vranesic, Fundamentals of Digital Logic with Verilog Design, Third Edition, McGraw Hill, 2014.
2.	Morris Mano and Michael D. Ciletti, Digital Design: With an Introduction to the Verilog HDL, Fifth Edition, Pearson Higher Education, 2013.

E-Resources

E1	https://docs.google.com/file/d/0B2om2B98SOeiLTY5WWNaSjh4bm8/edit?resourcekey=0-PFVlEteUUiXDSv8msJOGKg

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Programme	**M.E.**	Programme Code			**205**	Regulation		**2023**
Department	**VLSI DESIGN / ELECTRONICS AND COMMUNICATION ENGINEERING**				Semester			**II**
Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P23VD205	**Low Power VLSI Design**	3	0	0	3	40	60	100

Course Objective

The main objective of the course is

- To identify sources of power in an IC and principle of low power design.
- To identify the power optimization techniques based on different level of methods in CMOS
- To explore the concept of power optimization and estimation analysis.
- To understand the layout design and special techniques.
- To study the software design for low power techniques.

Course Outcome

At the end of the course, the student should be able to	Knowledge Level
CO1: Analyze different source of power dissipation and the factors involved	K4
CO2: Understand the different techniques involved in low power adders and multipliers	K3
CO3: Identify and analyze the different techniques involved in reducing power consumption in adders and multipliers	K3
CO4: Understand various power estimation techniques.	K2
CO5: Study different power optimization techniques in design of circuits.	K4

Pre-requisites -

CO / PO Mapping
(3/2/1 indicates strength of correlation) 3-Strong, 2 – Medium, 1 - Weak

CO/PSO Mapping

Cos	Programme Outcomes (POs)												PSOs		
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2	PSO 3
CO 1	3	3	2	2								1	3	2	
CO 2	3	3	2	2								1	3	2	
CO 3	3	3	2	2								1	3	2	
CO 4	3	3	2	2								1	3	2	
CO 5	3	2	2	2								1	3	2	

Course Assessment Methods

Direct

1. Continuous Assessment Test I, II & III
2. Assignment, Seminar and Quiz
3. End-Semester examinations

Indirect

1. Course – end survey

Content of the syllabus

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Unit – I	POWER DISSIPATION IN CMOS	Periods	9
Hierarchy of limits of power – Sources of power consumption – Physics of power dissipation in CMOS FET devices- Basic principle of low power design.			
Unit – II	**POWER OPTIMIZATION**	Periods	**9**
Logical level power optimization – Circuit level low power design – Gate Level Low Power Design – Architecture Level Low Power Design – VLSI Subsystem Design of Adders, Multipliers, PLL, Low Power Design			
Unit – III	**DESIGN OF LOW POWER CMOS CIRCUITS**	Periods	**9**
Computer Arithmetic techniques for low power systems – Reducing Power Consumption in Combinational Logic, Sequential Logic, Memories – Low Power Clock – Advanced Techniques – Special Techniques, Adiabatic Techniques – Physical Design, Floor Planning, Placement and Routing .			
Unit – IV	**POWER ESTIMATION**	Periods	**9**
Power Estimation Techniques, Circuit Level, Gate Level, Architecture Level, Behavioral Level, – Logic Power Estimation – Simulation Power Analysis –Probabilistic Power Analysis			
Unit – V	**SYNTHESIS AND SOFTWARE DESIGN FOR LOW POWER**	Periods	**9**
Synthesis for Low Power – Behavioral Level Transform –Algorithms for Low Power – Software Design for Low Power.			
		Total Periods	**45**

References

1.	K.Roy& S.C. Prasad, "Low Power CMOS VLSI Circuit Design" ,Wiley, 2009.
2.	DimitriosSoudris, ChirstianPignet, Costas Goutis, "Designing CMOS Circuits for Low Power",Kluwer Academic Publishers, 2002.
3.	J.B. Kuo and J.H Lou, "Low Voltage CMOS VLSI Circuits", Wiley 1999.
4.	A.P.Chandrakasan and R.W. Broadersen, "Low Power Digital CMOS Design", Kluwer Academic Publishers ,1995.
5.	Gary Yeap, "Practical Low Power Digital VLSI Design", Kluwer, 1998.
6.	AbdellatifBellaouar, Mohamed.I. Elmasry, "Low Power Digital VLSI Design", Kluwer Academic Publishers, 1995.
7.	James B. Kuo, Shin – chia Lin, "Low Voltage SOI CMOS VLSI Devices and Circuits",John Wiley & sons, Inc 2001.

E-Resources

E1	https://www.google.co.in/books/edition/Low_Power_Cmos_Vlsi_Circuit_Design/eQKCHEyJcewC?hl=en&gbpv=1&dq=low+power+vlsi+design&printsec=frontcover
E2	https://www.google.co.in/books/edition/Low_Power_Digital_VLSI_Design/0IfkBwAAQBAJ?hl=en&gbpv=1&dq=low+power+vlsi+design&printsec=frontcover
E3	https://www.google.co.in/books/edition/Low_Power_Design_Methodologies/9IzuBwAAQBAJ?hl=en&gbpv=1&dq=low+power+vlsi+design&printsec=frontcover

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Programme	**M.E.**	Programme Code	**205**	Regulation	**2023**			
Department	**VLSI DESIGN / ELECTRONICS AND COMMUNICATION ENGINEERING**			Semester	**II**			
Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P23VD206	**Testing and Verification of VLSI Circuits**	3	0	0	3	40	60	100

Course Objective

The main objective of the course is

- To study the fault modeling and detection techniques.
- To understand the test generation for combinational and sequential logic circuits.
- To explore the design for testability and self test methods.
- To study the fault diagnosis.
- To study the Timing verification of VLSI Circuits

Course Outcome	At the end of the course, the student should be able to	Knowledge Level
	CO1: Insert elementary testing hardware into the VLSI chip	K2
	CO2: Analyze VLSI circuit timing using Logical Effort analysis	K4
	CO3: Estimate and compute the power consumption of a VLSI chip	K3
	CO4: Understand the concept of test generation and simulation.	K2
	CO5: Design and Verify the VLSI Circuits.	K3

Pre-requisites -

CO / PO Mapping (3/2/1 indicates strength of correlation) 3-Strong, 2 – Medium, 1 - Weak													**CO/PSO Mapping**		
Cos	Programme Outcomes (POs)												PSOs		
	PO 1	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO 10**	**PO 11**	**PO 12**	**PSO 1**	**PSO 2**	**PSO 3**
CO 1	3	3	2	2									3	2	
CO 2	3	3	2	2									3	2	
CO 3	3	3	2	2									3	2	
CO 4	3	3	2	2									3	2	
CO 5	3	3	2	2									3	2	

Course Assessment Methods

Direct
1. Continuous Assessment Test I, II & III 2. Assignment, Seminar and Quiz 3. End-Semester examinations
Indirect
1. Course – end survey

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Content of the syllabus			
Unit – I	**FUNDAMENTALS OF TESTING**	Periods	**9**
Scope of testing and verification in VLSI design process. Issues in test and verification of complex chips, embedded cores and SOCs; Fundamentals of VLSI testing.			
Unit – II	**TEST GENERATION AND SIMLUATION**	Periods	**9**
Automatic test pattern generation. Design for testability. Scan design. Test interface and boundary scan. System testing and test for SOCs. Iddq testing.			
Unit – III	**FAULT MODELS**	Periods	**9**
Fault models: Delay fault testing. BIST for testing of logic and memories. Test automation.			
Unit – IV	**DESIGN AND VERIFICATION OF VLSI CIRCUITS**	Periods	**9**
Design verification techniques based on simulation, Analytical and Formal approaches. Functional verification of VLSI circuits.			
Unit – V	**TIMING VERIFICATION OF VLSI CIRCUITS**	Periods	**9**
Timing verification. Formal verification. Basics of equivalence checking and model checking. Hardware emulation.			
		Total Periods	**45**

References	
1.	M. Bushnell and V. D. Agrawal, "Essentials of Electronic Testing for Digital", Memory and Mixed-Signal VLSI Circuits", Kluwer Academic Publishers, 2004.
2.	M. Abramovici, M. A. Breuer and A. D. Friedman, "Digital Systems Testing and Testable Design", IEEE Press, 1990.
3.	T.Kropf, "Introduction to Formal Hardware Verification", Springer Verlag, 2000.
4.	P. Rashinkar, Paterson and L. Singh, "System-on-a-Chip Verification-Methodologyand Techniques", Kluwer Academic Publishers, 2001.
E-Resources	
E1	https://www.google.co.in/books/edition/Essentials_of_Electronic_Testing_for_Dig/UTrtBwAAQBAJ?hl=en&gbpv=1&dq=testing+and+verification+in+vlsi&printsec=frontcover
E2	https://www.google.co.in/books/edition/System_on_a_Chip_Verification/76wPBwAAQBAJ?hl=en&gbpv=1&dq=P.+Rashinkar,+Paterson+and+L.+Singh,+System-on-a-Chip+Verification-Methodologyand++Techniques&printsec=frontcover

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Programme	M.E.	Programme Code	205	Regulation	2023
Department	VLSI DESIGN / ELECTRONICS AND COMMUNICATION ENGINEERING			Semester	II

Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P23VD207	VLSI for Wireless Communication	3	0	0	3	40	60	100

Course Objective

The main objective of the course is

- To understand the basics of wireless communication.
- To understand the concepts of transceiver architectures.
- To introduce to the students the low power design techniques of VLSI circuits.
- To learn the design and implementation of various VLSI circuits for wireless communication systems.
- To learn the VLSI Design of synthesizers.

Course Outcome

At the end of the course, the student should be able to	Knowledge Level
CO1: Understand the application of VLSI circuits in wireless communication.	K2
CO2: Knowledge of various architectures used in implementing wireless systems.	K3
CO3: Design and simulation of low power techniques using software	K4
CO4: Learn the VLSI design of wireless circuits.	K2
CO5: Learnthe VLSI Design of synthesizers	K2

Pre-requisites Wireless Communication

CO / PO Mapping (3/2/1 indicates strength of correlation) 3-Strong, 2 – Medium, 1 - Weak — **CO/PSO Mapping**

Cos	Programme Outcomes (POs)												PSOs		
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2	PSO 3
CO 1	3	3	3	2						2			3		
CO 2	3	3	3	2					2	2			3		
CO 3	3	3	3	2					2				3	2	
CO 4	3	3	3	2									3	2	
CO 5	3	3	3	2										2	

Course Assessment Methods

Direct

1. Continuous Assessment Test I, II & III
2. Assignment, Seminar and Quiz
3. End-Semester examinations

Indirect

1. Course - end survey

Content of the syllabus

Unit – I	WIRELESS COMMUNICATION BASICS	Periods	9

Digital communication systems- minimum bandwidth requirement, Shannon limit- overview of

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modulation schemes- classical channel- wireless channel description- path loss- multipath fading- basics of spread spectrum and spread spectrum techniques- and Direct sequence			
Unit – II	**TRANSCEIVER ARCHITECTURE**	Periods	**9**
Transceiver design constraints- baseband subsystem design- RF subsystem design- Super heterodyne receiver and direct conversion receiver- Receiver front-end- filter design- non-idealities and design parameters- derivation of noise figure and IP3 of receiver front end.			
Unit – III	**LOW POWER DESIGN TECHNIQUES**	Periods	**9**
Source of power dissipation- estimation of power dissipation- reducing power dissipation at device and circuit levels- low voltage and low power operation- reducing power dissipation at architecture and algorithm levels			
Unit – IV	**WIRELESS CIRCUITS**	Periods	**9**
VLSI Design of LNA-wideband and narrow band-impedance matching. Automatic Gain Control (AGC) amplifier-power amplifier- Active mixer- analysis, conversion gain, distortion analysis- low frequency and high frequency case, noise. Passive mixer- sampling mixer and switching mixer- analysis of distortion, conversion gain and noise in these mixers.			
Unit – V	**VLSI DESIGN OF SYNTHESIZERS**	Periods	**9**
VLSI design of Frequency Synthesizers (FS) – Parameters of FS - PLL based frequency synthesizer, phase detector/charge pump- dividers- VCO- LC oscillators- ring oscillator- phase noise- loop filter- description design approaches			
		Total Periods	**45**

References	
1.	Bosco Leung, "VLSI for Wireless Communication", Springer, 2011.
2.	Elmad N Farag and Mohamed I Elmasry, "Mixed Signal VLSI Wireless Design-Circuits and Systems",Kluwer Academic Publishers, 2002.
E-Resources	
E1	https://nptel.ac.in/courses/117102062/CO-ORDINATED BY : IIT DELHI
E2	https://nptel.ac.in/courses/117102062/2CO-ORDINATED BY : IIT DELHI

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	VIVEKANANDHA COLLEGE OF ENGINEERING FOR WOMEN (Autonomous Institution, Affiliated to Anna University ,Chennai) Elayampalayam, Tiruchengode – 637 205							
Programme	**M.E.**	Programme Code	**205**	Regulation	**2023**			
Department	**VLSI DESIGN / ELECTRONICS AND COMMUNICATION ENGINEERING**			Semester	**II**			
Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P23VD208	**Digital VLSI System Laboratory**	0	0	4	2	60	40	100

Course Objective

The main objective of the course is

- To know and understand HDL and design circuits using it.
- To understand the design of various types of microcontroller(s)
- To analyze the power and timing of complex digital Circuits using EDA tools
- Obtain the layout of digital design using Cadence- Virtuoso
- To study this course the student will know basic electronics involved in the design of MOS circuits.

Course Outcome

At the end of the course, the student should be able to	Knowledge Level
CO1: Design of FIR Filter using EDA Tool.	K3
CO2: Analysis and design of VLSI circuits.	K3
CO3: Design of different types of multiplier using EDA Tool.	K3
CO4:Obtain the layout of digital design	K4
CO5: Design of Embedded System applications based on advanced Microcontrollers.	K4

Pre-requisites -

CO / PO Mapping (3/2/1 indicates strength of correlation) 3-Strong, 2 – Medium, 1 - Weak

CO/PSO Mapping

Cos	Programme Outcomes (POs)												PSOs		
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2	PSO 3
CO 1	3				3								3	2	
CO 2	3				3								3	2	
CO 3	3				3								3	2	
CO 4	3				3								3	2	
CO 5	3				3								3	2	

Course Assessment Methods

Direct
1. Pre lab and Post lab Test.
2. End-Semester examinations
Indirect
1. Course - end survey

Content of the syllabus

S.No	Suggested List of Experiments	CO Mapping

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HDL SIMULATION AND IMPLEMENTATION OF FPGA:		
1	Design and Implementation of 8 Bit ALU in FPGA / CPLD	CO1
2	Design and Implementation of Elevator controller using embedded microcontroller	CO2
3	Design and Implementation of Alarm clock controller using embedded microcontroller	CO2
4	Design and Implementation of model train controller using embedded microcontroller	CO2
5	Design and Simulation of FIR filter using HDL	CO1
BACK-END EDA TOOL EXPERIMENTS:		
6	Design and simulation of Multiplier using EDA Tools	CO3
7	Design and simulation of SRAM using EDA Tools	CO3
8	Design and simulation of Adders using Tanner EDA Tools	CO4
9	Mini project in CMOS digital circuits	CO5
	Total Periods	**45**

References	
1.	BehzadRazavi, "Design of Analog CMOS Integrated Circuits", Edition 2002, McGraw--Hill Edition reprint 2017.
2.	David A. Johns, Martin K, "Analog Integrated Circuit Design", John Wiley& Sons, Inc., New York, 2013.
E-Resources	
E1	ESim - EDA tool for circuit design, simulation, analysis and PCB design - Course (swayam2.ac.in)
E2	Digital Electronic Circuits - Course (nptel.ac.in)

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Programme	**M.E.**	Programme Code	**205**	Regulation	**2023**		
Department	**VLSI DESIGN / ELECTRONICS AND COMMUNICATION ENGINEERING**			Semester	**II**		
Course Code	Course Name	Periods Per Week			Credit	Maximum Marks	
		L	T	P	C	CA	ESE	Total
P23VD209	**VLSI Design Verification and Testing Laboratory**	0	0	4	2	60	40	100

Course Objective

The main objective of the course is

- To learn testing and verification in VLSI design process
- To implement and verify Finite State Machines using Verilog File I/O
- To study different types of TBs.
- To analyze the Verification Planning for FIFO/UART
- To write assertions for FIFO.

Course Outcome

At the end of the course, the student should be able to	Knowledge Level
CO1: Test and Verify VLSI design process.	K3
CO2: Implement and verify Finite State Machines using Verilog File I/O Design.	K2
CO3: Understand different types of TBs.	K2
CO4: Verify Planning for FIFO/UART.	K3
CO5: Write assertions for FIFO.	K2

Pre-requisites -

CO / PO Mapping (3/2/1 indicates strength of correlation) 3-Strong, 2 – Medium, 1 - Weak													CO/PSO Mapping		
Cos	Programme Outcomes (POs)												PSOs		
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2	PSO 3
CO 1	3	2	2	2	3				2				3	2	
CO 2	3	2	2	2	3				2				3	2	
CO 3	3	2	2	2	3				2				3	2	
CO 4	3	2	2	2	3				2				2	2	
CO 5	3	2	2	2	3				2				2	2	

Course Assessment Methods

Direct
1. Pre lab and Post lab Test.
2. End-Semester examinations
Indirect
1. Course - end survey

Content of the syllabus

S.No	Suggested List of Experiments	CO Mapping

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1	Verilog Simulation and RTL Verification a) Memory b) Clock Divider and Address Counter n-Bit Binary Counter and RTL Verification	CO1
2	Finite State Machines Implement and Verify Using Verilog File I/O.	CO2
3	Different types of TBs for memory and adder/subtractor.	CO3
4	Basic Verification environment for FIFO/UART.	CO2
5	Verification Planning for FIFO/UART a) Development of the test cases as per the verification plan b) Generation and Analysis of Code coverage Reports.	CO1
6	Writing assertions for FIFO.	CO5
7	Design and Verification of Ripple Carry Adder (Dataflow, Structural, Gate level, Behavioral, Test bench creation).	CO2
8	Gate level analysis of different stuck at faults in a CMOS Gate (NAND, NOR).	CO1
9	Design of a LFSR and calculate the different power dissipation for the circuit (8bit, 16bit, 32 bit) using BIST.	CO2
10	Perform timing analysis for a given sequential circuit.	CO4
	Total Periods	**45**

References	
1.	M. Bushnell and V. D. Agrawal, "Essentials of Electronic Testing for Digital", Memory and Mixed-Signal VLSI Circuits", Kluwer Academic Publishers, 2000.
2.	M. Abramovici, M. A. Breuer and A. D. Friedman, "Digital Systems Testing and Testable Design", IEEE Press, 1990.
3.	T.Kropf, "Introduction to Formal Hardware Verification", Springer Verlag, 2000.
4.	P. Rashinkar, Paterson and L. Singh, "System-on-a-Chip Verification-Methodology and Techniques", Kluwer Academic Publishers, 2001.
E-Resources	
E1	https://nptel.ac.in/courses/106103116/Prof.SanthoshBiswas
E2	https://www.elprocus.com/ripple-carry-adder-working-types-and-its-applications/
E3	https://3ec1218usm.files.wordpress.com/2016/12/book_systemverilog_for_verification.pdf

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Unit – I	INTRODUCTION TO ASICS, CMOS LOGIC ANDASIC LIBRARY DESIGN	Periods	9
Types of ASICs - Design flow - CMOS transistors CMOS Design rules - Combinational Logic Cell – Sequential logic cell - Data path logic cell - Transistors as Resistors - Transistor Parasitic Capacitance- Logical effort –Library cell design - Library architecture.			
Unit – II	**PROGRAMMABLE ASICS, PROGRAMMABLE ASIC LOGIC CELLS AND PROGRAMMABLE ASIC I/O CELLS**	Periods	**9**
Anti fuse - static RAM - EPROM and EEPROM technology - PREP benchmarks - Actel ACT - Xilinx LCA –Altera FLEX - Altera MAX DC & AC inputs and outputs - Clock & Power inputs - Xilinx I/O blocks.			
Unit – III	**PROGRAMMABLE ASIC INTERCONNECT, PROGRAMMABLE ASIC DESIGN SOFTWARE AND LOW LEVEL DESIGN ENTRY**	Periods	**9**
Actel ACT -Xilinx LCA - Xilinx EPLD - Altera MAX 5000 and 7000 - Altera MAX 9000 - Altera FLEX – Design systems - Logic Synthesis - Half gate ASIC -Schematic entry - Low level design language - PLA tools -EDIF- CFI design representation.			
Unit – IV	**LOGIC SYNTHESIS, SIMULATION AND TESTING**	Periods	**9**
Verilog and logic synthesis -VHDL and logic synthesis - types of simulation -boundary scan test - fault simulation - automatic test pattern generation.			
Unit – V	**ASIC CONSTRUCTION, FLOOR PLANNING, PLACEMENT AND ROUTING**	Periods	**9**
System partition - FPGA partitioning - partitioning methods - floor planning - placement - physical design flow –global routing - detailed routing - special routing - circuit extraction - DRC.			
		Total Periods	**45**

References	
1.	M.J.S .Smith, "Application - Specific Integrated Circuits", Addison -Wesley Longman Inc., 1997.
2.	Andrew Brown, " VLSI Circuits and Systems in Silicon", McGraw Hill, 1991
3.	S.D. Brown, R.J. Francis, J. Rox, Z.G. Uranesic, " Field Programmable Gate Arrays", Kluwer Academic Publishers, 1992.
4.	Mohammed Ismail and Terri Fiez, "Analog VLSI Signal and Information Processing", McGraw Hill, 1994.
5.	S. Y. Kung, H. J. Whilo House, T. Kailath, " VLSI and Modern Signal Processing", Prentice Hall,1985.
6.	Jose E. France, YannisTsividis, "Design of Analog - Digital VLSI Circuits for Telecommunicationand Signal Processing", Prentice Hall, 1994.
E-Resources	
E1	https://www.multisoftsystems.com/embedded-systems/asic-design-verification-training
E2	https://nptel.ac.in/courses/106106089/magma_tutorial/magma_tutorial.html

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Programme	**M.E.**	Programme Code	**205**	Regulation	**2023**			
Department	**VLSI DESIGN / ELECTRONICS AND COMMUNICATION ENGINEERING**			Semester	**III**			
Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P23VD311	**ASIC Design**	3	0	0	3	40	60	100

Course Objective

The main objective of the course is

- To study about ASIC fundamentals.
- To study different level of ASIC flow.
- To explore modeling of ASIC design.
- To study FPGA partitioning.
- To study about the ASIC construction, floor planning, placement and routing

Course Outcome	At the end of the course, the student should be able to	Knowledge Level
	CO1: Understand ASICS, CMOS logic and ASIC library design	K2
	CO2: Analyze altera MAX 9000	K4
	CO3: Analyze the VHDL and logic synthesis	K4
	CO4: Understand the ASIC construction	K2
	CO5: Know different kinds of routing in ASIC Design	K3

Pre-requisites CMOS VLSI

CO / PO Mapping (3/2/1 indicates strength of correlation) 3-Strong, 2 – Medium, 1 - Weak													**CO/PSO Mapping**		
Cos	Programme Outcomes (POs)												PSOs		
	PO 1	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO 10**	**PO 11**	**PO 12**	**PSO 1**	**PSO 2**	**PSO 3**
CO 1	3	3	3	2									3	3	
CO 2	3	3	3	2										2	
CO 3	3	3	3	2										2	
CO 4	3	3	3	2									3		
CO 5	3	3	2	2									3		

Course Assessment Methods

Direct
1. Continuous Assessment Test I, II & III 2. Assignment and Seminar 3. End-Semester examinations
Indirect
1. Course - end survey

Content of the syllabus

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Programme	**M.E.**	Programme Code	**205**	Regulation	**2023**		
Department	**VLSI DESIGN / ELECTRONICS AND COMMUNICATION ENGINEERING**			Semester	**I**		

Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P23VDE01	**Embedded System Design**	3	0	0	3	40	60	100

Course Objective

The main objective of the course is

- To study the overview of Embedded System Design life cycle
- To learn about the memory organization.
- To study the interfacing Concepts.
- To know about debugging tool.
- To study about various testing methods.

Course Outcome

At the end of the course, the student should be able to	Knowledge Level
CO1: Realize the design flow of Embedded systems	K2
CO2: Analyze partition decision and interrupt service routine	K4
CO3: Utilize basic tool set used for debugging software and hardware	K3
CO4: Analyze various in- circuit tool sets for debugging embedded hardware and memories	K3
CO5: Apply different testing methods involved in test phase for the design of embedded system	K3

Pre-requisites: Embedded systems

CO / PO Mapping (3/2/1 indicates strength of correlation) 3-Strong, 2 – Medium, 1 - Weak													CO/PSO Mapping		
Cos	Programme Outcomes (POs)												PSOs		
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2	PSO 3
CO 1	3	3	2	2						3			3	2	
CO 2	3	3	2	2						2			3	2	
CO 3	3	2	2	2									3	2	
CO 4	3	3	3	2									3	2	
CO 5	3	3	3	2						2			3	2	

Course Assessment Methods

Direct
1. Continuous Assessment Test I, II & III 2. Assignment, Seminar and Quiz 3. End-Semester examinations
Indirect
1. Course – end survey

Content of the syllabus

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Unit – I	EMBEDDED DESIGN LIFE CYCLE	Periods	09
Product specification – Hardware / Software partitioning – Detailed hardware and software design – Integration – Product testing – Selection Processes – Microprocessor Vs Micro Controller – Performance tools–Benchmarking–RTOSMicroController–Performancetools–Benchmarking–RTOSavailability – Tool chain availability – Other issues in selection processes.			
Unit – II	**PARTITIONING DECISION**	**Periods**	**09**
Hardware / Software duality – coding Hardware – ASIC revolution – Managing the Risk – Co-verification – execution environment – memory organization – System startup – Hardware manipulation – memory mapped access – speed and code density.			
Unit – III	**INTERRUPT SERVICE ROUTINES**	**Periods**	**09**
Watch dog timers – Flash Memory basic toolset – Host based debugging – Remote debugging – ROM emulators – Logic analyzer – Caches – Computer optimization – Statistical profiling.			
Unit – IV	**IN CIRCUIT EMULATORS**	**Periods**	**09**
Bullet proof run control – Real time trace – Hardware break points – Overlay memory – Timing constraints – Usage issues – Triggers.			
Unit – V	**TESTING**	**Periods**	**09**
Bug tracking – reduction of risks & costs – Performance – Unit testing – Regression testing – Choosing test cases – Functional tests – Coverage tests – Testing embedded software – Performance testing – Maintenance.			
		Total Periods	**45**

References

1.	Arnold S. Berger, "Embedded System Design", CMP books, USA 2017.
2.	Frank Vahid,Tony Givargis, "Embedded System Design-A Unified Hardware/Software Introduction",2018
3.	Embedded / Real-Time Systems: Concepts, Design and Programming, Dr. K.V.K Prasad,2013

E-Resources

E1	https://nptel.ac.in/courses/106105159/,Prof.anupambasu, IIT Kharagpur
E2	https://www.globalspec.com/reference/28434/203279/chapter-1-the-embedded-design-life-cycle#

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Programme	**M.E.**	Programme Code	**205**	Regulation	**2023**		
Department	**VLSI DESIGN / ELECTRONICS AND COMMUNICATION ENGINEERING**			Semester	**I**		

Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P23VDE02	**Physics of MOS Transistors**	3	0	0	3	40	60	100

Course Objective

The main objective of the course is

- To provide an in-depth knowledge in VLSI Design methodology.
- To enhance the fundamentals of different scaling rules.
- To study Small Signal Analysis
- To study NANO MOS transistors
- To study properties of optical receiver

Course Outcome	At the end of the course, the student should be able to	Knowledge Level
	CO1: Analyze a NANO MOS transistor model	K4
	CO2: Understand Scaling Rules for transistors structures	K2
	CO3: Design and analysis of circuits in different scaling.	K3,K6
	CO4: Analyze small signal transistor	K4
	CO5: Understand different optical properties	K2
Pre-requisites	EDC	

CO / PO Mapping (3/2/1 indicates strength of correlation) 3-Strong, 2 – Medium, 1 - Weak													**CO/PSO Mapping**		
Cos	Programme Outcomes (POs)												PSOs		
	PO 1	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO 10**	**PO 11**	**PO 12**	**PSO 1**	**PSO 2**	**PSO 3**
CO 1	3	3	2	2							2			3	
CO 2	3	3	2	2										3	
CO 3	3	3	3	3							2		2	3	
CO 4	3	3	3	2							2		3		
CO 5	3	3	3	2									2		

Course Assessment Methods

Direct
1. Continuous Assessment Test I, II & III 2. Assignment, Seminar and Quiz 3. End-Semester examinations
Indirect
1. Course - end survey

Content of the syllabus

Unit – I	**MOS TRANSISTORS**	Periods	**9**

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The MOS transistor: Pao-Sah and Brews models; Short channel effects in MOS transistors. Hot-carrier effects in MOS transistors; Quasi-static compact models of MOS transistors; Types of models for circuit Simulation, Measurement of MOS transistor parameters.			
Unit – II	**SCALING RULES**	Periods	**9**
Scaling and transistors structures for ULSI; Silicon-on-insulator transistors; High-field and radiation effects in transistors, The bipolar transistor.			
Unit – III	**SMALL SIGNAL ANALYSIS**	Periods	**9**
Ebers-Moll model; charge control model; small-signal and switching characteristics; Graded-base and graded- emitter transistors; High-current and high- frequency effects; Hetero junction bipolar transistors; Junction FETs; JFET, MESFET and hetero junction FET.			
Unit – IV	**NANO MOS TRANSISTOR**	Periods	**9**
Schrödinger equation, states and operators, particle-in-a-box, density-of-states, harmonic oscillator, hydrogen atom, tunneling, two-level systems. Electrons in a crystal lattice, quantum effects, Fundamental limits of MOS operations.			
Unit – V	**OPTICAL PROPERTIES**	Periods	**9**
Maxwell's equations in dielectric media, polarization in insulators, ferroelectrics, polarons and polaritons, direct and indirect transitions in semiconductors, excitons, optoelectronic and photovoltaic devices.			
		Total Periods	**45**

References

1.	R.M.Warner , B.L.Grung , " MOSFET – Theory and Design", Published by Oxford University Press, 1999.
2.	Yannis Tsividis, Colin Mc Andrew "Operation and Modeling of the MOS Transistor", Published by Oxford University Press, 2011.
3.	Simon M. Sze, Kwe K. Ng, "Physics of Semiconductor Devices", Wiley Eastern 3rd Edition, 2006.
4.	P.I.Varghese, T. Pradeep, A.Ashok Reddy, "A Text Book of Nanoscience and Nanotechnology" published by McGraw Hill Education 1st Edition, 2017.

E-Resources

E1	https://nptel.ac.in/courses/117102061/24CO-ORDINATED BY : IIT DELHI
E2	https://nptel.ac.in/courses/115102014/CO-ORDINATED BY : IIT DELHI

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Programme	**M.E.**	Programme Code	**205**	Regulation	**2023**		
Department	**VLSI DESIGN / ELECTRONICS AND COMMUNICATION ENGINEERING**			Semester	**I**		

Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P23VDE03	**Foundations of VLSI CAD**	3	0	0	3	40	60	100

Course Objective

The main objective of the course is

- To study the concepts and properties associated with graph theory.
- To learn the basics of physical design process such as partitioning and placement.
- To analyze the different types of floor planning, placement and routing algorithms.
- To learn the two level logic synthesis and binary decision diagrams.
- To learn the synthesis in VLSI physical design automation.

Course Outcome

At the end of the course, the student should be able to	Knowledge Level
CO1: Understand the design methodologies of VLSI and graph analysis	K4
CO2: Analyze the physical design process of VLSI design flow process	K4
CO3: Interpret the concepts of physical design process such as routing and floor planning	K5
CO4: Describe the concepts of simulation in VLSI physical design automation	K3
CO5: Understand the modeling and synthesis of VLSI physical design automation	K2

Pre-requisites

CO / PO Mapping (3/2/1 indicates strength of correlation) 3-Strong, 2 – Medium, 1 - Weak													**CO/PSO Mapping**		
Cos	Programme Outcomes (POs)												PSOs		
	PO 1	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO 10**	**PO 11**	**PO 12**	**PSO 1**	**PSO 2**	**PSO 3**
CO 1	3	3	2	3										2	
CO 2	3	3	2	3								2		2	
CO 3	3	3	2	3						2		2	3	2	
CO 4	3	3	2	2						2			3		
CO 5	3	2	2	2						2			3		

Course Assessment Methods

Direct

1. Continuous Assessment Test I, II & III
2. Assignment, Seminar and Quiz
3. End-Semester examinations

Indirect

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1. Course – end survey			
Content of the syllabus			
Unit – I	**VLSI DESIGN METHODOLOGIES**	Periods	**9**
Introduction to VLSI Design methodologies – Review of Data structures and algorithms –Review of VLSI Design automation tools – Algorithmic Graph Theory and Computational Complexity – Tractable and Intractable problems – general purpose methods for combinatorial optimization.			
Unit – II	**DESIGN RULES**	Periods	**9**
Layout Compaction – Design rules – problem formulation – algorithms for constraint graph compaction – placement and partitioning – Circuit representation – Placement algorithms – partitioning.			
Unit – III	**FLOOR PLANNING**	Periods	**9**
Floor planning concepts – shape functions and Floor plan sizing – Types of local Routing problems – Area routing – channel routing – global routing – algorithms for global routing.			
Unit – IV	**SIMULATION**	Periods	**9**
Simulation – Gate-level Modeling and simulation – Switch-level modeling and and simulation-Combinational Logic Synthesis – Binary Decision Diagrams – Two Level Logic Synthesis.			
Unit – V	**MODELLING AND SYNTHESIS**	Periods	**9**
High level Synthesis – Hardware models – Internal representation – Allocation –assignment and scheduling – Simple scheduling algorithm – Assignment problem – High level transformations.			
		Total Periods	**45**
Text Books			
1.	S.H. Gerez, "Algorithms for VLSI Design Automation", John Wiley & Sons,2002		
2.	N.A. Sherwani, "Algorithms for VLSI Physical Design Automation", Kluwer Academic Publishers, 2002.		
Reference Book:			
1.	Sarafzadeh, C.K. Wong, "An Introduction to VLSI Physical Design", McGraw Hill International Edition 1995		
E-Resources			
E1	https://nptel.ac.in/courses/108102042/CO-ORDINATED BY : IIT DELHI		
E2	https://nptel.ac.in/courses/106102062/ CO-ORDINATED BY : IIT DELHI		

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	VIVEKANANDHA COLLEGE OF ENGINEERING FOR WOMEN (Autonomous Institution, Affiliated to Anna University ,Chennai) Elayampalayam, Tiruchengode – 637 205						
Programme	**M.E.**	Programme Code	**205**	Regulation	**2023**		
Department	**VLSI DESIGN / ELECTRONICS AND COMMUNICATION ENGINEERING**			Semester	**I**		
Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P23VDE04	**HDL with System modeling.**	3	0	0	3	40	60	100

Course Objective

The main objective of the course is

- To understand the Concepts of Hardware Description Language.
- To study the Concepts of Statements and Programming of VHDL and Verilog HDL.
- To understand the Concepts of Timing Issues and System Modeling in HDL.
- To understand the Concepts timing issues and Processor model in VHDL
- To understand the Concepts of System Verilog

Course Outcome

At the end of the course, the student should be able to	Knowledge Level
CO1:Use hardware description language to design and simulate digital circuits using data flow and behavioral modeling	K2
CO2: Analyze of logic circuits by using different levels of modeling using VHDL	K3
CO3: Write the Verilog Program for logic circuits and synthesis by using tech bench	K3
CO4:Analyze the timing issues and Processor models	K4
CO5: Understand the basic concepts of System Verilog	K2

Pre-requisites: Digital System Design

CO / PO Mapping (3/2/1 indicates strength of correlation) 3-Strong, 2 – Medium, 1 - Weak												**CO/PSO Mapping**		
Cos	Programme Outcomes (POs)											PSOs		
	PO 1	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO 10**	**PO 11**	**PO 12**	**PSO 1**	**PSO 2**	**PSO 3**
CO 1	3	3	3	2							2		3	2	3
CO 2	3	3	3		2						2		3	2	3
CO 3	3	3	3	2	2						2	2	3	2	3
CO 4	3	3	3	2								2		2	3
CO 5	3	3	3	2	2								3	2	3

Course Assessment Methods

Direct

1. Continuous Assessment Test I, II & III
2. Assignment, Seminar and Quiz
3. End-Semester examinations

Indirect

1. Course - end survey

Content of the syllabus

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Unit – I	**BASIC CONCEPTS OF HARDWARE DESCRIPTIONLANGUAGE**	**Periods**	**9**
Comparison between HDL and High Level Language Hierarchy, Concurrency, Logic and Delay Modeling,Structural, Data flow, Behavioral Styles of Hardware Description, Architecture of event driven simulation			
Unit – II	**VHDL**	**Periods**	**9**
Data Types, Operators, Classes of Objects, entities and architectures, Attributes – concurrent statements – sequential statements – signals and variables – Behavior, dataflow and structural modeling – Configurations, functions –procedures – packages – test benches – Design examples			
Unit – III	**VERILOG**	**Periods**	**9**
Signals, Identifier Names, Net and Variable Types, operators, Gate instantiations, Verilog module, concurrent and procedural statements, UDP, sub circuit parameters, function and tasks – test benches – Design Examples			
Unit – IV	**TIMING ISSUES**	**Periods**	**9**
Modeling delay, timing modeling, timing modeling, timing assertion, setup and hold times for clocked devices, Processor model, RAM model, UART model			
Unit – V	**SYSTEM VERILOG**	**Periods**	**9**
Data Types: Built-in Data Types, Fixed-Size Arrays, Dynamic Arrays, Queues, Creating New Types With Typedef, Creating User-Defined Structures, Enumerated Types, Constants, Strings. Procedural Statements and Routines: Procedural Statements, Tasks, Functions, and Void Functions			
		Total Periods	**45**

References	
1.	Samir Palnitkar, "Verilog HDL: A Guide to Digital Design and Synthesis", 2nd Edition, Pearson Education New Delhi, 2019
2.	J.Bhasker Prime, —A Verilog HDL r, Prentice Hall, 2018
3.	Chris Spear, "System Verilog for Verification: A Guide to Learning the Test bench Language Features", 2nd Edition, Springer, 2012
4.	J.Bhasker, —A VHDL Primer, Prentice Hall, 1998.
5.	J.Bhasker, —VHDL Synthesis Primer, Prentice Hall.1998
6.	J.Bhasker, —A Verilog Primer, Prentice Hall 2005.
7.	Michel D Ciletti, —Advanced Digital Design with Verilog HDL, Pearson education, 2010.
8.	Neil Weste and Kamran Eshranghian, —Principles of CMOS VLSI Design, Addison Wesley, 2000.

E-Resources	
E1	https://nptel.ac.in/courses/117101004/17CO-ORDINATED BY : IIT BOMBAY
E2	https://nptel.ac.in/courses/117101004/downloads/Lecture%20Notes/D.K.%20Sharma/L17.pdf
E3	https://archive.nptel.ac.in/courses/106/105/106105165/:IIT KHARAGPUR
E4	https://d1.amobbs.com/bbs_upload782111/files_33/ourdev_585395BQ8J9A.pdf

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	VIVEKANANDHA COLLEGE OF ENGINEERING FOR WOMEN (Autonomous Institution, Affiliated to Anna University ,Chennai) Elayampalayam, Tiruchengode – 637 205						
Programme	M.E.	Programme Code	205	Regulation	2023		
Department	VLSI DESIGN / ELECTRONICS AND COMMUNICATION ENGINEERING			Semester	I		
Course Code	Course Name	Periods Per Week			Credit	Maximum Marks	
		L	T	P	C	CA	ESE	Total
P23VDE05	Introduction to MEMS	3	0	0	3	40	60	100

Course Objective

The main objective of the course is

- To study the basics concepts of MEMS and Micromachining.
- To attain the concepts of Microsystems Design techniques and MicroSensors.
- To analyse the concepts of Microactuator systems
- To acquire sound knowledge about Mechanical MEMS.
- To study the concepts Optical MEMS

Course Outcome	At the end of the course, the student should be able to	Knowledge Level
	CO1: Understand the materials used in MEMS and Micromachining processes.	K2
	CO2: Analyze etching methods and the various models of micro sensors	K4
	CO3: Explore various Micro actuator systems.	K2
	CO4: Design Mechanical MEMS	K3
	CO5: Interpret optical MEMS system	K2

Pre-requisites -

CO / PO Mapping (3/2/1 indicates strength of correlation) 3-Strong, 2 – Medium, 1 - Weak													CO/PSO Mapping		
Cos	Programme Outcomes (POs)												PSOs		
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2	PSO 3
CO 1	3	3	3	2			2			3				2	
CO 2	3	3	3	2			2			3				2	
CO 3	3	3	3	2			2						3	2	
CO 4	3	3	3	2			2						3		
CO 5	3	3	2	2			2						3		

Course Assessment Methods

Direct
1. Continuous Assessment Test I, II & III 2. Assignment, Seminar and Quiz 3. End-Semester examinations
Indirect
1. Course - end survey

Content of the syllabus

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Unit – I	MEMS FUNDAMENTALS	Periods	9
Historical Background: Resonant gate transistor (RGT), Silicon Pressure sensors, Micromachining, Micro Electro Mechanical Systems. Micro fabrication and Micromachining : Integrated Circuit Processes, Bulk Micromachining.			
Unit – II	**ETCHING METHODS & SENSORS**	Periods	**9**
Isotropic Etching and Anisotropic Etching, Wafer Bonding, High Aspect-Ratio Processes (LIGA);Physical Micro sensors : Classification of physical sensors, Integrated, Intelligent, or Smart sensors, Sensor Principles and Examples : Thermal sensors, Electrical Sensors, Mechanical Sensors, Chemical and Biosensors.			
Unit – III	**MICRO ACTUATORS**	Periods	**9**
Micro actuators: Electromagnetic and Thermal micro actuation, Mechanical design of micro actuators, Micro actuator examples, micro valves, micro pumps, Micromotors- Microactuator systems: Ink-Jet printer heads, Micro-mirror TV Projector.; Surface Micromachining: One or two sacrificial layer processes, Surface micromachining requirements.			
Unit – IV	**MECHANICAL MEMS**	Periods	**9**
Poly silicon surface micromachining, Other compatible materials, Silicon Dioxide, Silicon Nitride, Piezoelectric materials, Surface Micro machined Systems : Micro motors, Gear trains, Mechanisms.; Application Areas: All-mechanical miniature devices, 3-D electromagnetic actuators and sensors.			
Unit – V	**OPTICAL MEMS**	Periods	**9**
RF/Electronics devices, Optical/Photonic devices, Medical devices e.g. DNA-chip, micro-arrays.; lab/Design:(two groups will work on one of the following design project as a part of the course),Optical/Photonic device/system, Medical device e.g. DNA-chip, micro-arrays. Optical Switches			
		Total Periods	**45**

References

1.	Tai Ran Hsu, -MEMS & Micro Systems Design and Manufacture, Tata McGraw Hill, New Delhi, 21st reprint 2014
2.	P.Rai-Choudhury - MEMS and MOEMS Technology and Applications, SPIE Press, 2009
3.	Stephen Santuria, - Microsystems Design, Kluwer publishers, Springer US, 2005.
4.	NadimMaluf, - An introduction to Micro electro Mechanical System Design, Artech House,2004
5.	Mohamed Gad-el-Hak, The MEMS Handbook, CRC press Baco Raton, 2002

E-Resources

E1	https://nptel.ac.in/courses/117105082/CO-ORDINATED BY : IIT KHARAGPUR
E2	https://ocw.mit.edu/courses/6-777j-design-and-fabrication-of-microelectromechanical-devices-spring-2007/
E3	https://www.coursera.org/learn/sensor-manufacturing-process-control

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Programme	**M.E.**	Programme Code	**205**	Regulation	**2023**			
Department	**VLSI DESIGN / ELECTRONICS AND COMMUNICATION ENGINEERING**			Semester	**I**			
Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P23VDE06	**Multimedia Compression Techniques**	3	0	0	3	40	60	100

Course Objective

The main objective of the course is

- To explore the special features and representations of different data types.
- To analyze different compression techniques for text data and audio signals
- To analyze various compression techniques for image and video signals.

Course Outcome

At the end of the course, the student should be able to	Knowledge Level
CO1: Use Compression techniques in multimedia.	K2
CO2: Know different text compression techniques and its application.	K3
CO3: Learn the concept of various audio compression methods.	K4
CO4: Identify various image compression techniques.	K4
CO5: Learn the concept of various video compression techniques and its application.	K2

Pre-requisites -

CO / PO Mapping (3/2/1 indicates strength of correlation) 3-Strong, 2 – Medium, 1 - Weak													CO/PSO Mapping		
Cos	Programme Outcomes (POs)												PSOs		
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2	PSO 3
CO 1	3	3	3	2	2					2		2	3		
CO 2	3	3	3	2									3		
CO 3	3	3	3	2									3	2	
CO 4	3	3	3	2									3	2	
CO 5	3	3	3	2										2	

Course Assessment Methods

Direct
1. Continuous Assessment Test I, II & III 2. Assignment, Seminar and Quiz 3. End-Semester examinations
Indirect
1. Course - end survey

Content of the syllabus

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Unit – I	**INTRODUCTION**	Periods	**9**
Special features of Multimedia – Graphics and Image Data Representations – Fundamental Concepts in Text, Images, Graphics, Video and Digital Audio – Storage requirements for multimedia applications - Need for Compression – Taxonomy of compression techniques –Error free Compression-Lossy Compression.			
Unit – II	**TEXT COMPRESSION**	Periods	**9**
Compression techniques – Huffman coding – adaptive Huffman coding – arithmetic coding – Shannon- Fano coding – dictionary techniques –LZ77, LZ78, LZW family algorithms.			
Unit – III	**AUDIO COMPRESSION**	Periods	**9**
Audio compression techniques - μ- Law and A- Law companding - Frequency domain and filtering – Basic sub- band coding –Speech coding standard-G.722-Audio coding standard MPEG audio, progressive encoding for audio – Silence compression techniques.			
Unit – IV	**IMAGE COMPRESSION**	Periods	**9**
Image compression: Fundamentals-compression standards-JPEG Standard – Sub-band coding algorithms - Wavelet based compression -Implementation using filters – EZW, SPIHT coders – JPEG2000 standards - JBIG, JBIG2 standards- Run length coding.			
Unit – V	**VIDEO COMPRESSION**	Periods	**9**
Video compression techniques and standards – MPEG Video Coding I: MPEG – 1 and 2 – MPEG Video Coding II -MPEG – 4 and 7 – Motion estimation and compensation techniques – H.261 Standard – DVI technology – DVI real time compression – Packet Video.			
		Total Periods	**45**
References			
1.	Khalid Sayood,"Introduction to Data Compression", Morgan Kauffman Harcourt India, Fourth Edition, 2012		
E-Resources			
E1	www.ics.uci.edu/~dan/pubs/DataCompression.html		
E2	https://nptel.ac.in/courses/106105082/38CO-ORDINATED BY : IIT KHARAGPUR		
E3	https://nptel.ac.in/downloads/117105083/CO-ORDINATED BY : IIT KHARAGPUR		
FURTHER READINGS:			
1	IEEE Transactions on "Information Theory".		
2	http://www.arturocampos.com/compression.html		

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Programme	**M.E.**	Programme Code	**205**	Regulation	**2023**		
Department	**VLSI DESIGN / ELECTRONICS AND COMMUNICATION ENGINEERING**			Semester	**I**		
Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P23VDE07	**Semiconductor Memory Design**	3	0	0	3	40	60	100

Course Objective

The main objective of the course is

- To acquire knowledge about different types of semiconductor memories.
- To study about architecture and operations of different semiconductor memories.
- To comprehend the semiconductor memory reliability.
- To study the semiconductor memory radiation effects.
- To study the advanced memory technology.

Course Outcome

At the end of the course, the student should be able to	Knowledge Level
CO1: Analyze the different types of RAM, ROM designs.	K4
CO2: Analyze the different RAM and ROM architecture and interconnects.	K4
CO3: Analyze the semiconductor memory reliability.	K4
CO4: Analyze the radiation effects of semiconductor memories.	K3
CO5: Identify the new developments in semiconductor memory design.	K3

Pre-requisites EC-I & II

CO / PO Mapping
(3/2/1 indicates strength of correlation) 3-Strong, 2 – Medium, 1 - Weak

CO/PSO Mapping

Cos	Programme Outcomes (POs)												PSOs		
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2	PSO 3
CO 1	3	3	2	2						2			3	2	
CO 2	3	3	2	2						2				2	
CO 3	3	3	2	2						2				2	
CO 4	3	3	2	2							3		3		
CO 5	3	3	2	2							3		3		

Course Assessment Methods

Direct

1. Continuous Assessment Test I, II & III
2. Assignment, Seminar and Quiz
3. End-Semester examinations

Indirect

1. Course - end survey

Content of the syllabus

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Unit – I	**RANDOM ACCESS MEMORY TECHNOLOGIES**	Periods	**9**
Static Random Access Memories (SRAM): SRAM cell structure, MOS SRAM Architecture, MOS SRAM cell and peripheral Circuit Operation, Bipolar SRAM Technologies, Silicon on Insulator (SOI) technology. Advanced SRAM Architectures and Technologies, Application Specified SRAMs. Dynamic Random access Memories (DRAM): DRAM Technology Development, CMOS DRAM, DRAM cell theory and advanced cell structure, BiCMOS DRAM, soft error failure in DRAM, Advanced DRAM Design and Architecture, Application Specific DRAM			
Unit – II	**NON- VOLATILE MEMORIES**	Periods	**9**
Masked Read only Memories (ROM), High density ROMs, Programmable ROM, Bipolar ROMs, CMOS PROMs, Erasable (UV) programmable ROM (EPROM), Floating, Gate EPROM cell, one time programmable EPROM (OTPEPROM), Electrically Erasable PROMS, EEPROM Technology and architecture, Non Volatile SRAM, Flash Memories (EPROM and EEPROM), Advance flash memory Architecture			
Unit – III	**SEMICONDUCTOR MEMORY RELIABILITY**	Periods	**9**
General Reliability issue- RAM Failure modes and Mechanism- nonvolatile memory Reliability- Reliability modeling and failure rate prediction- Design for reliability – Reliability test structure- reliability screening and qualification.			
Unit – IV	**SEMICONDUCTOR MEMORY RADIATION EFFECTS**	Periods	**9**
Single Event Phenomenon (SEP). Radiation Hardening Technique- Radiation hardening process and design issue- radiation hardened memory characteristics — Radiation hardness assurance and testing.			
Unit – V	**ADVANCED MEMORY TECHNOLOGY**	Periods	**9**
Ferroelectric Random Access Memories (FRAMs) – Gallium Arsenide (GaAs) FRAMs – Analog Memories- Magneto resistive RAMs (MRAMs) - Experimental memory device.			
		Total Periods	**45**

References	
1.	Ashok K Sharna, "Semiconductor Memories Technology", Testing and Reliability, Wiley 2002.
2.	Ashok K Sharna, "Advanced Semiconductor Memories–Architecture, Design and Applications",Wiley2002.
3.	AnjanGhosh, "High Speed Semiconductor Devices", NPTEL Courseware, 2009.
E-Resources	
E1	http://www.bitsavers.org/pdf/ti/_Texas_Instruments_Electronics_Series/Luecke_Semiconductor_Memory_Design_and_Application_1973.pdf
E2	https://archive.nptel.ac.in/courses/117/101/117101058/
E3	https://books.google.co.in/books/about/Semiconductor_Memories.html?id=VNsmAQAAMAAJ&redir_esc=y

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Programme	**M.E.**	Programme Code		**205**	Regulation		**2023**	
Department	**VLSI DESIGN / ELECTRONICS AND COMMUNICATION ENGINEERING**				Semester		**I**	
Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P23VDE08	**System on Chip Design**	3	0	0	3	40	60	100

Course Objective

The main objective of the course is

- To understand the concepts of SOC design issues.
- To understand the concepts of SOC Design methodology for Logic Cores.
- To understand the concepts of System on Chip Design methodology for memory and analog Cores.
- To understand the concepts of System on Chip Design Validation.
- To understand the concepts of SOC Testing.

Course Outcome

At the end of the course, the student should be able to	Knowledge Level
CO1: Understand the concepts of System on Chip Design methodology for Logic and Analog Cores.	K2
CO2: Understand the concepts of SOC Design methodology for memory	K2
CO3: Comprehend System on Chip Design Validation methods	K4
CO4: Analyze SOC with various testing	K4
CO5: Analyze various types of testing	K4

Pre-requisites -

CO / PO Mapping (3/2/1 indicates strength of correlation) 3-Strong, 2 – Medium, 1 - Weak													CO/PSO Mapping		
Cos	Programme Outcomes (POs)												PSOs		
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2	PSO 3
CO 1	3	3	3	2					2				3		
CO 2	3	3	2	2					2			2	3		
CO 3	3	3	3	2					2				3	2	
CO 4	3	3	2	2						2				2	
CO 5	3	3	3	2						2				2	

Course Assessment Methods

Direct

1. Continuous Assessment Test I, II & III
2. Assignment, Seminar and Quiz
3. End-Semester examinations

Indirect

1. Course - end survey

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Content of the syllabus			
Unit – I	**INTRODUCTION**	Periods	**9**
System tradeoffs and evolution of ASIC Technology- System on chip concepts and methodology – SOC design issues -SOC challenges and components.			
Unit – II	**DESIGN METHODOLOGICAL FOR LOGIC CORES**	Periods	**9**
SOC Design Flow – On-chip buses –Design process for hard cores –Soft and firm cores –Designing with hardcores, soft cores- Core and SOC design examples.			
Unit – III	**DESIGN METHODOLOGY FOR MEMORY AND ANALOG CORES**	Periods	**9**
Embedded memories –Simulation modes Specification of analog circuits – A to D converter –Phase- located loops –High I/O.			
Unit – IV	**DESIGN VALIDATION**	Periods	**9**
Core level validation –Test benches –SOC design validation – Co simulation –hardware/ Software co-verification. Case Study: Validation and test of systems on chip.			
Unit – V	**SOC TESTING**	Periods	**9**
SOC Test Issues – Testing of digital logic cores –Cores with boundary scan –Test methodology for design reuse– Testing of microprocessor cores – Built in self method –testing of embedded memories. Case Study: Integrating BIST techniques for on-line SOC testing.			
		Total Periods	**45**

References	
1.	Rochit Rajsunah, "System-on-a-Chip: Design and Test", Artech House, 2007.
2.	Prakash Raslinkar, Peter Paterson &Leena Singh, "System-on-a-Chip Verification: Methodology and Techniques", Kluwer Academic Publishers, 2000.
3.	M.Keating, D.Flynn, R.Aitken, A, GibbonsShi, "Low Power Methodology Manual for System-on-Chip Design Series: Integrated Circuits and Systems", Springer, 2007.
4.	L.Balado, E. Lupon, "Validation and Test of Systems on Chip", IEEE conference on SIC/SOC, 1999.
5.	A.Manzone, P.Bernardi, M.Grosso, M. Rebaudengo, E. Sanchez, M.SReorda, Centro Ricerche Fiat, "Integrating BIST Techniques for On-line SoC Testing", IEEE Symposium on On-Line testing, 2005.
E-Resources	
E1	https://nptel.ac.in/courses/108102045/10 CO-ORDINATED BY : IIT DELHI
E2	https://nptel.ac.in/courses/108102045/29CO-ORDINATED BY : IIT DELHI

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Programme	M.E.	Programme Code	205	Regulation	2023		
Department	VLSI DESIGN / ELECTRONICS AND COMMUNICATION ENGINEERING			Semester	-		
Course Code	Course Name	Periods Per Week			Credit	Maximum Marks	
		L	T	P	C	CA	ESE	Total
P23VDE09	Hardware Design Verification Techniques	3	0	0	3	40	60	100

Course Objective

The main objective of the course is

- To understand the Concepts of Verification Techniques and Tools.
- To study the concepts of Verification Plan,
- To study the concepts of Stimulus and Response.
- To understand the concepts of Architecting Test benches and System Verilog.
- To impart in-depth knowledge about RTL design.

Course Outcome

At the end of the course, the student should be able to	Knowledge Level
CO1: Analyze and design small scale combinational logic circuits using HDLs.	K4
CO2: Analyze the problems in digital design using HDLs.	K4
CO3: View VLSI design from a hierarchical view point.	K2
CO4: Select appropriate analysis for circuit design.	K3
CO5: Analyze architecting Test Benches.	K4

Pre-requisites

CO / PO Mapping (3/2/1 indicates strength of correlation) 3-Strong, 2 – Medium, 1 - Weak												CO/PSO Mapping		
Cos	Programme Outcomes (POs)												PSOs		
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2	PSO 3
CO 1	3	3	3	2									3	2	
CO 2	3	3	3	2									3	2	
CO 3	3	3	3	2									3	2	
CO 4	3	3	3	2											
CO 5	3	3	3	2											

Course Assessment Methods

Direct

1. Continuous Assessment Test I, II & III
2. Assignment and Seminar
3. End-Semester examinations

Indirect

1. Course - end survey

Content of the syllabus

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Unit – I	VERIFICATION TECHNIQUES AND TOOLS	Periods	9
Testing vs. Verification – Verification and Design Reuse - Functional Verification, Timing Verification, Formal Verification, Linting Tools – Simulators – Third Party Models – Waveform Viewers – Code Coverage issue–Tracking Metrics.			
Unit – II	**VERIFICATION PLAN**	Periods	**9**
Verification plan – Levels of Verification – Verification Strategies – Specification Features – Test cases – Test Benches			
Unit – III	**STIMULUS AND RESPONSE**	Periods	**9**
Simple Stimulus – Output Verification – Self Checking Test Benches – Complex Stimulus and Response –Prediction of Output			
Unit – IV	**ARCHITECTING TEST BENCHES**	Periods	**9**
Reusable Verification Components – VHDL and Verilog Implementation – Autonomous Generation and Monitoring– Input and Output Paths — Verifying Configurable Design.			
Unit – V	**SYSTEM VERILOG**	Periods	**9**
Data types, RTL design, Interfaces, clocking, Assertion based verification, classes, Test bench Automations and constraints.			
		Total Periods	**45**

References

1.	Janick Bergeron, "Writing Test Benches Functional Verification of HDL Models", Springer, 2003.
2.	Andreas Meyer, "Principles of Functional Verification", Newnes, 2004.
3.	Samir Palnitkar, "Design Verification with E", Prentice Hall, 2003.
4.	T.Kropf, "Introduction to Formal Hardware Verification", Springer Verlag, 2010.
5.	Chris Spear, " System Verilog for Verification: A Guide to Learning the Test bench Language Features", Springer,2008
6.	Janick Bergeron, Edward Cerny, Alan Hunter and Andrew Nightingale, "Verification Methodology Manual for System Verilog", Springer, 2005.

E-Resources

E1	https://www.oreilly.com/library/view/hardware-design-verification/0131433474/
E2	https://faculty.sist.shanghaitech.edu.cn/faculty/songfu/cav/Lam05.pdf

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Programme	M.E.	Programme Code	205	Regulation	2023		
Department	VLSI DESIGN / ELECTRONICS AND COMMUNICATION ENGINEERING			Semester	-		
Course Code	Course Name	Periods Per Week			Credit	Maximum Marks	
		L	T	P	C	CA	ESE	Total
P23VDE10	RF Microelectronics Chip Design	3	0	0	3	40	60	100

Course Objective

The main objective of the course is

- To study Resonator-less VCO.
- To study Linearization techniques.
- To understand the operation of MOS devices.
- To learn the basics of Multiple Access techniques
- To study about low noise amplifiers and mixers.

Course Outcome

At the end of the course, the student should be able to	Knowledge Level
CO1: Design various types of oscillators used in chip design	K3
CO2: Explain various features of low noise amplifiers.	K2
CO3: Sketch the Layout of simple transceiver architectures	K5
CO4: Microelectronics chip designing knowledge skills get improved	K4
CO5: Understand communication concepts in multiple access techniques.	K2

Pre-requisites

CO / PO Mapping (3/2/1 indicates strength of correlation) 3-Strong, 2 – Medium, 1 - Weak												CO/PSO Mapping		
Cos	Programme Outcomes (POs)												PSOs		
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2	PSO 3
CO 1	3	3	2	2					2				3		
CO 2	3	3	2	2					2				3		
CO 3	3	3	2	2					2				3	2	
CO 4	3	3	2	2						2	2			2	
CO 5	3	3	2							2				2	

Course Assessment Methods

Direct
1. Continuous Assessment Test I, II & III 2. Assignment and Seminar 3. End-Semester examinations
Indirect
1. Course – end survey

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Unit – I	BASIC CONCEPTS IN RF DESIGN	Periods	9
Complexity – design and applications, Choice of Technology, Basic concepts in RF Design –Non linearly and Time Variance – inter-symbol Interference – random processes and Noise, Definitions of sensitivity and dynamic range – conversion Gains and Distortion.			
Unit – II	**COMMUNICATION CONCEPTS**	Periods	**9**
Analog and Digital Modulation for RF circuits – Comparison of various techniques for power efficiency, Mobile RF Communication systems and basics of Multiple Access techniques.			
Unit – III	**RECEIVER AND TRANSCEIVER ARCHITECTURES**	Periods	**9**
Receiver and Transmitter Architectures and Testing heterodyne, Homodyne, Image-reject, Direct-IF and sub- sampled receivers. Direct Conversion and two steps transmitters, BJT and MOSFET behavior at RF frequencies Modeling of the transistors and SPICE models, Noise performance and limitation of devices. Transceiver Architecture and Design Example with Different Communication Modulations/Demodulations, Considerations			
Unit – IV	**LOW NOISE AMPLIFIERS AND MIXERS**	Periods	**9**
Basic blocks in RF systems and their VLSI implementation- Low Noise Amplifiers design in various technologies, Design of Mixers at GHz frequency range, Various Mixers, their working and implementations.			
Unit – V	**OSCILLATORS**	Periods	**9**
Cross Coupled oscillator, three point oscillator, voltage controlled oscillator – Low-noise VCO topologies-LC VCOs with wide tuning range, Phase noise, Design procedures.			
		Total Periods	**45**

References

1.	T.Lee, "Design of CMOS RF Integrated Circuits", Cambridge, 2004.
2.	Sorin Voinigescu "High-Frequency Integrated Circuits," Cambridge University press, 2013,
3.	B.Razavi, "RF Microelectronics", Pearson Education, 1997.
4.	Jan Crols, MichielSteyaert, "CMOS Wireless Transceiver Design", Kluwer Academic Publishers,1997.
5.	B.Razavi, "Design of Analog CMOS Integrated Circuits", McGraw Hill, 2001.

E-Resources

E1	https://nptel.ac.in/courses/117102012/,course co-ordinated by IIT Delhi.

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Programme	**M.E.**	Programme Code	**205**	Regulation	**2023**		
Department	**VLSI DESIGN / ELECTRONICS AND COMMUNICATION ENGINEERING**			Semester	-		

Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P23VDE11	**Mixed Signal VLSI Design**	3	0	0	3	40	60	100

Course Objective	The main objective of the course is • To understand the types of filters. • To understand the different techniques of ADC and DAC. • To focus on Submicron CMOS process flow • To gain knowledge on data converters. • To understand concepts of switched capacitor filters.

Course Outcome	At the end of the course, the student should be able to	Knowledge Level
	CO1: Use DAC and ADC techniques for data conversions.	K2
	CO2: Program, Mixed Signal VLSI Circuits.	K3
	CO3: Understand various signal conversion techniques.	K2
	CO4: Identify and analyze the different techniques involved in mixed signal VLSI design	K4
	CO5: Understand concepts of switched capacitor filters	K2

Pre-requisites

CO / PO Mapping (3/2/1 indicates strength of correlation) 3-Strong, 2 – Medium, 1 - Weak												CO/PSO Mapping		
Cos	Programme Outcomes (POs)												PSOs		
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2	PSO 3
CO 1	3	3	3	2						2			3	2	
CO 2	3	3	3	2						2			3	2	
CO 3	3	3	3	2						2			3	2	
CO 4	3	3	3	2								2	3		
CO 5	3	3	3	2								2	3		

Course Assessment Methods

Direct
1. Continuous Assessment Test I, II & III 2. Assignment and Seminar 3. End-Semester examinations
Indirect
1. Course - end survey

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Unit – I	INTRODUCTION AND BASIC MOS DEVICES	Periods	9
Challenges in analog design-Mixed signal layout issues- MOSFET structures and characteristics-large signal model – small signal model- single stage Amplifier-Source follower- Common gate stage – Cascode Stage.			
Unit – II	**SUBMICRON CIRCUIT DESIGN**	Periods	9
Submicron CMOS process flow, Capacitors and resistors, Current mirrors, Digital Circuit Design, Delay Elements – Adders- OP Amp parameters and Design.			
Unit – III	**DATA CONVERTERS**	Periods	9
Characteristics of Sample and Hold- Digital to Analog Converters- architecture-Differential Non linearity-Integral Non linearity-Voltage Scaling-Cyclic DAC-Pipeline DAC-Analog to Digital Converters- architecture – Flash ADC-Pipeline ADC-Differential Non linearity-Integral Non linearity.			
Unit – IV	**SNR IN DATA CONVERTERS**	Periods	9
Overview of SNR of Data Converters- Clock Jitters- Improving Using Averaging – Decimating Filters for ADC- Band pass and High Pass Sinc Filters- Interpolating Filters for DAC.			
Unit –V	**SWITCHED CAPACITOR CIRCUITS**	Periods	9
Resistors, First order low pass Circuit, Switched capacitor Amplifier, Switched Capacitor Integrator Interconnects, Phase locked loops, Delay locked loops.			
		Total Periods	**45**

References	
1.	VineethaP.Gejji, "Analog and Mixed Mode Design" , Prentice Hall, 1st Edition , 2011
2.	JeyaGowri, "Analog and Mixed Mode Design",Sapna Publishing House 2011.
3.	R. Jacob Baker , "CMOS Mixed-signal circuit design", Wiley India, IEEE press, reprint 2008.
E-Resources	
E1	https://nptel.ac.in/syllabus/117101006/Prof.D.K.Sharma
E2	https://nptel.ac.in/courses/117101006/CO-ORDINATED BY : IIT BOMBAY
FURTHER READINGS:	
1.	Rudy V. Deplassche , "CMOS Integrated ADCs and DACs", Springer, Indian edition, 2005
2.	BehzadRazavi ,"Design of analog CMOS integrated circuits", McGraw-Hill, 2003

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Programme	**M.E.**	Programme Code	**205**	Regulation	**2023**
Department	**VLSI DESIGN / ELECTRONICS AND COMMUNICATION ENGINEERING**			Semester	-

Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P23VDE12	**Nano Electronics**	3	0	0	3	40	60	100

Course Objective

The main objective of the course is

- To acquire knowledge about fundamental quantum mechanics.
- To study about architecture and operations of different nanostructures.
- To comprehend the low dimension, high speed and low power design techniques and methodologies.
- To study photonic networks.
- To study about the data transmission, interfaces and Displays in Nano Electronics

Course Outcome

At the end of the course, the student should be able to	Knowledge Level
CO1: Comprehend fundamental quantum mechanics.	K4
CO2: Study about architecture and operations of different Nano structures.	K2
CO3: Comprehend the low dimension, high speed and low power design techniques and methodologies.	K4
CO4: Understand data transmission techniques.	K2
CO5: Study about the data transmission, interfaces and Displays in Nano Electronics	K2

Pre-requisites VLSI design and circuits, Semiconductor materials

CO / PO Mapping
(3/2/1 indicates strength of correlation) 3-Strong, 2 – Medium, 1 - Weak

CO/PSO Mapping

Cos	Programme Outcomes (POs)												PSOs		
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2	PSO 3
CO 1	3	3	2	2									3		
CO 2	3	3	2	2				2					3		
CO 3	3	3	3	2				2					3		
CO 4	3	3	3	2				2					3	2	
CO 5	3	3	3	2										2	

Course Assessment Methods

Direct

1. Continuous Assessment Test I, II & III
2. Assignment and Seminar
3. End-Semester examinations

Indirect

1. Course – end survey

Content of the syllabus

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Unit – I	TECHNOLOGY AND ANALYSIS	Periods	9
Film Deposition Methods – Lithography- Material removing techniques – Etching and Chemical-Mechanical Polishing – Scanning Probe Techniques.			
Unit – II	**CARBON NANO STRUCTURES**	Periods	**9**
Carbon Clusters – Carbon Nano tubes – Fabrication – Electrical, Mechanical and Vibrational Properties – Applications of Carbon Nano tubes.			
Unit – III	**LOGIC DEVICES**	Periods	**9**
Silicon MOSFET's – Novel materials and alternative concepts – Ferroelectric Field Effect Transistors – Super conductor digital electronics – Carbon Nano tubes for data processing.			
Unit – IV	**RANDOM ACCESS MEMORIES AND MASS STORAGE DEVICES**	Periods	**9**
High Permittivity material for DRAM's – Ferro electric Random Access memories – Magneto- resistive RAM- Hard Disk Drives – Magneto Optical Disks – Rewriteable DVDs based on Phase Change Materials – Holographic Data Storage.			
Unit – V	**DATA TRANSMISSION AND INTERFACES AND DISPLAYS**	Periods	**9**
Photonic Networks – Microwave Communication System – Liquid Crystal Displays – Organic Light emitting diodes.			
		Total Periods	**45**

References

1.	Rainer Waser, "Nano Electronics and Technology", Wiley VCH, 2003.
2.	Charles Poole, "Introduction to Nano Technology", Wiley Inter science, 2003.
3.	C.Wasshuber, Simon , "Simulation of Nano Structures Computational Single-Electronics", Springer-Velag, 2001.
4.	Rainer Waser, "Nano Electronics and information technology advanced electronic materials and novel devices", Wiley –VcHVerlagGmBh-KgaH, Germany, 2005.
5.	**M.** Mark Reed and Takhee Lee, "Molecular Nano Electronics", American Scientific Publisher, California, 2003.

E-Resources

E1	https://ocw.mit.edu/courses/electrical-engineering-and-computer-science/6-701-introduction-to-nanoelectronics
E2	https://nptel.ac.in/courses/117108047/, Course Co-ordinated By : IISC Bangalore

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Programme	**M.E.**	Programme Code	**205**	Regulation	**2023**		
Department	**VLSI DESIGN / ELECTRONICS AND COMMUNICATION ENGINEERING**			Semester	-		
Course Code	Course Name	Periods Per Week			Credit	Maximum Marks	
		L	T	P	C	CA	ESE	Total
P23VDE13	**Processors and Embedded Controllers**	3	0	0	3	40	60	100

Course Objective

The main objective of the course is

- To understand Basics of Microprocessor Architecture ,Instruction set, Data formats
- To understand RISC and CISC architecture and evaluation
- To acquire knowledge about ARM processors and CPU cores.
- To understand the concepts of 32 bit Free scale Cold Fire Processors and Programming skills.
- To understand the concept of Ethernet and CAN interfacing

Course Outcome

At the end of the course, the student should be able to	Knowledge Level
CO1: Analyze the different types of Architectures	K4
CO2: Learn about instruction Set for different architectures	K5
CO3: Understand and analysis about the Assembly language Program for various industry based applications	K2
CO4: Apply knowledge in c programming with code warrior tools to analysis the functions of peripherals in Cold fire processor	K3
CO5: Understand Tools and software related to interfacing	K2

Pre-requisites

CO / PO Mapping (3/2/1 indicates strength of correlation) 3-Strong, 2 – Medium, 1 - Weak												CO/PSO Mapping		
Cos	Programme Outcomes (POs)											PSOs		
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2	PSO 3
CO 1	3	3	3	2							2	2	3	3	
CO 2	3	3	3	2									2	2	
CO 3	3	3	3	2									3		
CO 4	3	3	3	2										2	
CO 5	3	3	2	2										2	

Course Assessment Methods

Direct

1. Continuous Assessment Test I, II & III
2. Assignment and Seminar
3. End-Semester examinations

Indirect

1. Course – end survey

Content of the syllabus

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Unit – I	**MICROPROCESSOR ARCHITECTURE**	**Periods**	**9**
Instruction set – Data formats – Instruction formats – Addressing modes – Memory hierarchy – register file Cache –Virtual memory and paging – Segmentation – Pipelining – The instruction pipeline – pipeline Hazards Instruction level parallelism – reduced instruction set – Computer principles – RISC versus CISC RISC properties – RISC evaluation – On-chip register files versus cache evaluation			
Unit – II	**HIGH PERFORMANCE CISC ARCHITECTURE :PENTIUM**	**Periods**	**9**
The software model – functional description – CPU pin descriptions – RISC concepts – bus operations – Super scalar architecture – pipe lining – Branch prediction – The instruction and caches – Floating point unit–protected mode operation – Segmentation – paging – Protection – multitasking – Exception and interrupts–Input /Output – Virtual 8086 model – Interrupt processing –Instruction types – Addressing modes –Processor flags– Instruction set-programming the Pentium processor.			
Unit – III	**HIGH PERFORMANCE RISC ARCHITECTURE: ARM**	**Periods**	**9**
The ARM architecture – ARM assembly language program – ARM organization and implementation – The ARM instruction set – The thumb instruction set – ARM CPU cores.			
Unit – IV	**FREE SCALE COLDFIRE 32 BIT PROCESSOR**	**Periods**	**9**
Introduction to ColdFire Core, User and Supervisor Programming Model, Addressing modes, Special instructions, Exceptions and Interrupt controller, EMAC, - TheMCF5223X Microprocessor- The 5223X Microprocessor, SDRAM controller,Flex CAN, Fast Ethernet Controller USB.			
Unit – V	**FREE SCALE COLDFIRE 32 BIT ROCESSOR, PROGRAMMING**	**Periods**	**9**
Tools and Software – Interfacing SDRAM and Flash to Cold Fire Processor - UART, USB, Ethernet and CAN interfacing – C programming examples with Code Warrior tools.			
		Total Periods	**45**

References	
1.	Daniel Tabak, "Advanced Microprocessors", McGraw Hill,2001.
2.	L. James Antonakos, "The Pentium Microprocessor", Pearson Education, 2000
3.	MunirBannaoura, Rudan Bettelheim and Richard Soja, "ColdFire Microprocessors and Microcontrollers", AMT Publishing 2007
4.	Steve Furber, "ARM System –On Chip Architecture", Addison Wesley, 2000
5.	S.P. Das, "Microcontrollers and Applications", NPTEL Courseware, 2004.

E-Resources	
E1	https://swayam.gov.in/
E2	https://www.youtube.com/watch?v=cevi6eWMVdE

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Programme	**M.E.**	Programme Code		**205**	Regulation		**2023**	
Department	**VLSI DESIGN / ELECTRONICS AND COMMUNICATION ENGINEERING**				Semester		-	
Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P23VDE14	**Digital System Design with FPGA**	3	0	0	3	40	60	100

Course Objective

The main objective of the course is

- To study PLDs and system design concepts.
- To understand the concept of PCB Design and Design Languages.
- To study about Digital Logic Design with VHDL & Verilog.
- To study the general concepts in Testing.
- To study the system level Design with case study.

Course Outcome

At the end of the course, the student should be able to	Knowledge Level
CO1: Identify the various challenges in CPLD and FPGA	K2
CO2: Understand and recognize PCB design techniques and design languages used for system design.	K2
CO3: Understand to write hardware coding using VHDL& Verilog.	K2
CO4: Analyze testing of electronic systems.	K4
CO5: Designing of circuits for various projects using FPGA	K3

Pre-requisites

CO / PO Mapping (3/2/1 indicates strength of correlation) 3-Strong, 2 – Medium, 1 - Weak												**CO/PSO Mapping**		
Cos	Programme Outcomes (POs)											PSOs		
	PO 1	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO 10**	**PO 11**	**PO 12**	**PSO 1**	**PSO 2**	**PSO 3**
CO 1	3	3	2	2									2	2	
CO 2	3	3											3	2	
CO 3	3	3	2	3									2	2	
CO 4	3	3			2								2	2	
CO 5	3	3	2										2	2	

Course Assessment Methods

Direct
1. Continuous Assessment Test I, II & III 2. Assignment and Seminar 3. End-Semester examinations
Indirect
1. Course - end survey

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Unit – I	**PROGRAMMABLE LOGIC DEVICES & SYSTEM DESIGN CONCEPTS**	Periods	**9**
Introduction- History of Digital Logic- Programmable Logic versus Discrete Logic - Types of Programmable Logic -PLD Configuration Technologies - Programmable Logic Vendors – Programmable Logic Design Methods and Tools - Technology Trends.System Design: Sequential Product Development Process versus Concurrent Engineering Process- Gajski-Kuhn Chart- Hardware-Software Co-Design- Electronic System-Level Design - Digital Input/Output- Parallel and Serial Interfacing- System Reset-System Clock- Power Supplies- Power Management- System on a Chip and System in a Package.			
Unit – II	**PCB DESIGN & DESIGN LANGUAGES**	Periods	**9**
Introduction-PCB concept- Design, Manufacture, and Testing- Environmental Issues- Case Study PCB Designs -Technology Trends. Design Languages: Software Programming Languages- Hardware Description Languages- SPICE-System C–System Verilog- Mathematical Modeling Tools.			
Unit – III	**DIGITAL LOGIC DESIGN WITH VHDL AND VERILOG**	Periods	**9**
Introduction to VHDL& Verilog- Combinational Logic Design- Sequential Logic Design- Memories-Unsigned versus Signed Arithmetic- Testing the Design: Test Bench.			
Unit – IV	**TESTING THE ELECTRONIC SYSTEM**	Periods	**9**
Introduction- Integrated Circuit Testing- Printed Circuit Board Testing- Boundary Scan Testing-Software Testing.			
Unit – V	**SYSTEM LEVEL DESIGN**	Periods	**9**
Introduction- Electronic System-Level Design- Arithmetic Circuit Designs-Traffic light controller-Real time clock. Case Study 1: DC Motor Control- Case Study 2: Digital Filter Design- Automating the Translation.			
		Total Periods	**45**

References

1.	Ion Grout, "Digital Systems Design with FPGAs and CPLDs", Elsevier, 2008.
2.	SeetharamanRamachandran "Digital VLSI systems Design", Springer 2007.
3.	Cemunsala& bora Tar,"Digital System Design with FPGA : Implementation Using VHDL and Verilog,Mc-Graw Hill 2017
4.	Samir Palnitkar, "Verilog HDL", Pearson Education, 2nd Edition, 2004.
5.	W.Wolf, "FPGA- based System Design", Pearson, 2004

E-Resources

E1	https://swayam.gov.in/
E2	https://www.youtube.com/watch?v=k2xJtdLM50c

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Programme	**M.E.**	Programme Code	**205**	Regulation	**2023**
Department	**VLSI DESIGN / ELECTRONICS AND COMMUNICATION ENGINEERING**			Semester	--

Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P23VDE15	**Speech and Audio Signal Processing**	3	0	0	3	40	60	100

Course Objective

The main objective of the course is

- To study basic concepts of processing speech and audio signals
- To study and analyze various M-band filter-banks for audio coding
- To understand audio coding based on transform coders.
- To study time and frequency domain speech processing methods
- To study the predictive analysis of speech using various algorithms

Course Outcome

At the end of the course, the student should be able to	Knowledge Level
CO1: Study the fundamental concepts of speech and audio signals.	K2
CO2: Analyze various M-band filter-banks for audio coding.	K4
CO3: Understand audio coding based on transform coders.	K2
CO4: Study time and frequency domain speech processing methods	K2
CO5: Understand the predictive analysis of speech using various algorithms	K2

Pre-requisites

CO / PO Mapping
(3/2/1 indicates strength of correlation) 3-Strong, 2 – Medium, 1 - Weak

CO/PSO Mapping

Cos	Programme Outcomes (POs)												PSOs		
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2	PSO 3
CO 1	3	3	3	2									3		
CO 2	3	3	3	2									3	2	
CO 3	3	3	3	2									3	2	
CO 4	3	3	3	2										2	
CO 5	3	3	3	2										2	

Course Assessment Methods

Direct

1. Continuous Assessment Test I, II & III
2. Assignment and Seminar
3. End-Semester examinations

Indirect

1. Course – end survey

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Unit – I	MECHANICS OF SPEECHANDAUDIO	Periods	9
Introduction – Review of Signal Processing Theory-Speech production mechanism – Nature of Speech signal – Discrete time Modeling of Speech production – Classification of Speech sounds – Phones – Phonemes – Phonetic and Phonemic alphabets – Articulatory features. Absolute Threshold of Hearing Critical Bands- Simultaneous Masking, Masking-Asymmetry, and the Spread of Masking- Non-simultaneous Masking – Perceptual Entropy – Basic measuring philosophy –Subjective versus objective perceptual testing – The perceptual audio quality measure (PAQM) – Cognitive effects in judging audio quality.			
Unit – II	**TIME-FREQUENCY ANALYSIS: FILTER BANKSANDTRANSFORMS**	Periods	**9**
Introduction – Analysis-Synthesis Framework for M-band Filter Banks- Filter Banks for Audio Coding: Design Considerations – Quadrature Mirror and Conjugate Quadrature Filters – Tree-Structured QMF and CQF M-band Banks – Cosine Modulated "Pseudo QMF" M-band Banks –Cosine Modulated Perfect Reconstruction (PR) M-band Banks and the Modified Discrete Cosine Transform (MDCT) – Discrete Fourier and Discrete Cosine Transform – Pre-echo Distortion- Pre-echo Control Strategies			
Unit – III	**AUDIO CODING ANDTRANSFORM CODERS**	Periods	**9**
Lossless Audio Coding – Lossy Audio Coding – ISO-MPEG-1A, 2A, 2A-Advaned, 4A Audio Coding – Optimum Coding in the Frequency Domain – Perceptual Transform Coder –Brandenburg – Johnston Hybrid Coder – CNET Coders – Adaptive Spectral Entropy Coding –Differential Perceptual Audio Coder – DFT Noise Substitution –DCT with Vector Quantization –MDCT with Vector Quantization			
Unit – IV	**TIME AND FREQUENCY DOMAIN METHODS FORSPEECHPROCESSING**	Periods	**9**
Time domain parameters of Speech signal – Methods for extracting the parameters :Energy, Average Magnitude – Zero crossing Rate – Silence Discrimination using ZCR and energy Short Time Fourier analysis – Formant extraction – Pitch Extraction using time and frequency domain methods Homomorphic Speech Analysis: Cepstral analysis of Speech – Formant and Pitch Estimation – Homomorphic Vocoders			
Unit – V	**PREDICTIVE ANALYSISOFSPEECH**	Periods	**9**
Formulation of Linear Prediction problem in Time Domain – Basic Principle – Auto correlation method – Covariance method – Solution of LPC equations – Cholesky method – Durbin"s Recursive algorithm – lattice formation and solutions – Comparison of different methods – Application of LPC parameters – Pitch detection using LPC parameters – Formant analysis – VELP – CELP			
		Total Periods	**45**

References

1.	Ben Gold, Nelson Morgan, Dan Ellis, "Speech and Audio Signal Processing: Processing and Perception of Speech and Music", Wiley and Sons, 2011.
2.	L.R.Rabiner and R.W.Schaffer, "Digital Processing of Speech Signals", Prentice Hall, 2003.
3.	Mark Kahrs, Karlheinz Brandenburg, Kluwer,"Applications of Digital Signal Processing to Audio and Acoustics", Academic Publishers
4.	Udo Zölzer, "Digital Audio Signal Processing", Second Edition, A John Wiley& sons Ltd

E-Resources

E1	https://nptel.ac.in/courses/117105145/, Course Co-ordinated By : IIT Kharagpur
E2	http://homes.esat.kuleuven.be/~dspuser/dasp/material.html

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Programme	M.E.	Programme Code	205	Regulation	2023
Department	VLSI DESIGN / ELECTRONICS AND COMMUNICATION ENGINEERING		Semester		--

Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P23VDE16	**Internet of Things and Applications**	3	0	0	3	40	60	100

Course Objective

The main objective of the course is

- To understand the fundamentals of Internet of Things
- To learn about the basics of IOT protocols
- To build a small low cost embedded system using Raspberry Pi.
- To apply the concept of Internet of Things in the real world scenario
- To Analyze applications of IoT in real time scenario

Course Outcome	At the end of the course, the student should be able to	Knowledge Level
	CO1: Analyze various protocols for IoT	K4
	CO2: Develop web services to access/control IoT devices.	K3
	CO3: Design a portable IoT using Rasperry Pi	K3
	CO4: Deploy an IoT application and connect to the cloud.	K3
	CO5: Analyze applications of IoT in real time scenario	K4

Pre-requisites

CO / PO Mapping (3/2/1 indicates strength of correlation) 3-Strong, 2 – Medium, 1 - Weak													CO/PSO Mapping		
Cos	Programme Outcomes (POs)												PSOs		
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2	PSO 3
CO 1	3	3	2	2									3		
CO 2	3	3	2	2									3	2	
CO 3	3	3	2	2									3	2	
CO 4	3	3	2	2									3	2	
CO 5	3	3	2	2										2	

Course Assessment Methods

Direct

1. Continuous Assessment Test I, II & III
2. Assignment and Seminar
3. End-Semester examinations

Indirect

1. Course - end survey

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Content of the syllabus			
Unit – I	**INTRODUCTION TO IoT**	Periods	**9**
Internet of Things - Physical Design- Logical Design- IoT Enabling Technologies - IoT Levels & Deployment Templates - Domain Specific IoTs - IoT and M2M - IoT System Management with NETCONF-YANG- IoT Platforms Design Methodology			
Unit – II	**IoT ARCHITECTURE**	Periods	**9**
M2M high-level ETSI architecture - IETF architecture for IoT - OGC architecture - IoT reference model - Domain model - information model - functional model - communication model - IoT reference architecture			
Unit – III	**IoT PROTOCOLS**	Periods	**9**
Protocol Standardization for IoT – Efforts – M2M and WSN Protocols – SCADA and RFID Protocols – Unified Data Standards – Protocols – IEEE 802.15.4 – BACNet Protocol – Modbus– Zigbee Architecture – Network layer – 6LowPAN - CoAP– Security.			
Unit - IV	**BUILDING IoT WITH RASPBERRY PI , FPGA & ARDUINO**	Periods	**9**
Building IOT with RASPERRY PI- IoT Systems - Logical Design using Python – IoT Physical Devices & Endpoints - IoT Device -Building blocks -Raspberry Pi -Board - Linux on Raspberry Pi - Raspberry Pi Interfaces -Programming Raspberry Pi with Python - Actel ACT -Xilinx LCA - Xilinx EPLD - Altera MAX 5000 and 7000 - Altera MAX 9000 - Altera FLEX –Arduino.			
Unit - V	**CASE STUDIES AND REAL-WORLD APPLICATIONS**	Periods	**9**
Real world design constraints - Applications - Asset management, Industrial automation, smart grid, Commercial building automation, Smart cities - participatory sensing - Data Analytics for IoT – Software & Management Tools for IoT Cloud Storage Models & Communication APIs - Cloud for IoT - Amazon Web Services for IoT.			
		Total Periods	**45**
References			
1.	ArshdeepBahga, Vijay Madisetti, "Internet of Things – A hands-on approach", Universities Press, 2015		
2.	Dieter Uckelmann, Mark Harrison, Michahelles, Florian (Eds), "Architecting the Internet of Things", Springer, 2011.		
3.	Honbo Zhou, "The Internet of Things in the Cloud: A Middleware Perspective", CRC Press, 2012.		
4.	Jan Ho¨ ller, VlasiosTsiatsis , Catherine Mulligan, Stamatis , Karnouskos, Stefan Avesand. David Boyle, "From Machine-to-Machine to the Internet of Things - Introduction to a New Age of Intelligence", Elsevier, 2014.		
5.	Olivier Hersent, David Boswarthick, Omar Elloumi , "The Internet of Things – Key applications and Protocols", Wiley, 2012		
E-Resources			
E1	https://nptel.ac.in/courses/108108098/4CO-ORDINATED BY : IISC BANGALORE		
E2	https://nptel.ac.in/courses/106105166/CO-ORDINATED BY : IIT KHARAGPUR		

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Programme	**M.E.**	Programme Code	**205**	Regulation	**2023**			
Department	**VLSI DESIGN / ELECTRONICS AND COMMUNICATION ENGINEERING**			Semester	--			
Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P23VDE17	**Soft Computing**	3	0	0	3	40	60	100

Course Objective

The main objective of the course is

- To learn the key aspects of soft computing and Neural networks.
- To study the fuzzy logic components
- To understand the concept of optimization techniques.
- To gain insight onto Neuro Fuzzy modeling and control.
- To know about the components and building block hypothesis of Genetic algorithm.

Course Outcome	At the end of the course, the student should be able to	Knowledge Level
	CO1: Summarize the basic concepts of soft computing and Neural networks.	K2
	CO2: Classify Fuzzy set and solve Fuzzy problems.	K3
	CO3: Identify the various soft computing problems and solve using optimization techniques.	K3
	CO4: Categorize and compress the data using clustering algorithm and Feedback control	K3
	CO5: Write Genetic Algorithm to solve the optimization problem	K2

Pre-requisites

CO / PO Mapping (3/2/1 indicates strength of correlation) 3-Strong, 2 – Medium, 1 - Weak													**CO/PSO Mapping**		
Cos	Programme Outcomes (POs)												PSOs		
	PO 1	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO 10**	**PO 11**	**PO 12**	**PSO 1**	**PSO 2**	**PSO 3**
CO 1	3	3	3	2									3	2	
CO 2	3	3	3	2									3	3	
CO 3	3	3	3	2									3	3	
CO 4	3	3	2	2										2	
CO 5	3	3	2	2										3	

Course Assessment Methods

Direct
1. Continuous Assessment Test I, II & III 2. Assignment and Seminar 3. End-Semester examinations
Indirect
1. Course - end survey

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Content of the syllabus			
Unit – I	**BASICS OF SOFT COMPUTING AND NEURAL NETWORKS**	Periods	**9**
Evolution of Computing: Soft Computing Constituents, From Conventional AI to Computational Intelligence. Evolution of Neural Networks – Basic Models of ANN – Weights – Bias – Threshold – Learning Rate – Momentum Factor – Vigilance Parameter – McCulloch – Pitts Neuron – Linear Separability – Hebb Network.			
Unit – II	**FUZZY SET THEORY**	Periods	**9**
Fuzzy sets-Introduction, MF Formulation and parameterization, Fuzzy rules and Fuzzy reasoning-Extension principle, Fuzzy relations, If-Then rules and reasoning Fuzzy Interference systems-Mamdani, Sugeno, Tsukamoto Fuzzy models.			
Unit – III	**OPTIMIZATION**	Periods	**9**
Derivative based optimization-Descent methods, Method of steepest descent, Classical Newton's method, Step-size determination; Derivative free optimization- Genetic algorithm, Simulated annealing, Random search, Downhill search.			
Unit – IV	**ADVANCED NEURO-FUZZY MODELLING**	Periods	**9**
Classification and regression trees-Decision tress, Cart algorithm-Data clustering algorithms: K- means clustering, Fuzzy C-means clustering, Mountain clustering, Subtractive clustering-Rulebase structure identification- Nuero Fuzzy control.			
Unit – V	**GENETIC ALGORITHM**	Periods	**9**
Biological Background – Traditional Optimization and Search Techniques – Genetic Algorithm and Search Space – Simple GA – General Genetic Algorithm – Operators – Stopping Condition – Constraints.			
		Total Periods	**45**

References	
1.	JangJ.S.R.,SunC.TandMizutaniE,"NeuroFuzzyandSoftcomputing",Pearson education (Singapore) 2012.
FURTHER READINGS:	
1.	N.P.Padhy, —Artificial Intelligence and Intelligent Systems‖, Oxford University Press, 2011.
2.	Timothy J.Ross, —Fuzzy Logic with Engineering Applications‖, McGraw-Hill, 2011.
3.	Elaine Rich & Kevin Knight, —Artificial Intelligence, Second Edition‖, Tata Mcgraw Hill Publishing Comp., New Delhi,2006
4.	Timothy J.Ross, "Fuzzy Logic Engineering Applications", McGrawHill,NewYork,1997
E-Resources	
E1	http://www.cs.rpi.edu/courses/fall01/soft-computing/
E2	https://nptel.ac.in/courses/106105173/, Course Co-ordinated by : IIT Kharagpur

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Programme	M.E.	Programme Code	205	Regulation	2023
Department	VLSI DESIGN / ELECTRONICS AND COMMUNICATION ENGINEERING			Semester	--

Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P23VDE18	Networks on Chip	3	0	0	3	40	60	100

Course Objective

The main objective of the course is

- To learn the basic concepts of NoC design by studying the topologies.
- To identify the types of fault and study the testing methods for fault rectification.
- To study the Energy and Power Issues in NoC.
- To learn the different architecture design for on chip networks..
- To study the on chip communication and protocols of 3D NoC.

Course Outcome

At the end of the course, the student should be able to	Knowledge Level
CO1: Understand the concept of Routing Strategies	K2
CO2: Analyze the fault tolerance of NoC	K4
CO3: Analyze Energy and Power Issues in NoC	K4
CO4: Comprehend the energy and fault tolerance of NoC	K4
CO5: Understand the three dimensional networks-on-chip architectures	K2

Pre-requisites

CO / PO Mapping (3/2/1 indicates strength of correlation) 3-Strong, 2 – Medium, 1 - Weak													CO/PSO Mapping		
Cos	Programme Outcomes (POs)												PSOs		
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2	PSO 3
CO 1	3	3	3	2									3		
CO 2	3	3	3	2									3	3	
CO 3	3	3	3	2									3	3	
CO 4	3	3	2	2									2	2	
CO 5	3	3	2	2											

Course Assessment Methods

Direct

1. Continuous Assessment Test I, II & III
2. Assignment and Seminar
3. End-Semester examinations

Indirect

1. Course – end survey

Content of the syllabus

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Unit – I	INTRODUCTION TO NOC	Periods	9
Introduction to Network layers and Network Architecture; Interconnection Networks in Network-on-Chip- Network topologies - Switching Techniques - Routing Strategies - Flow Control Protocol Quality-of-Service Support.			
Unit – II	**TEST AND FAULT TOLERANCE OF NOC**	Periods	**9**
Design-Security in Networks-on-Chips-Formal Verification of Communications in Networks-on-Chips Test and Fault Tolerance for Networks-on-Chip Infrastructures-Monitoring Services for Networks-on Chips.			
Unit – III	**ENERGY AND POWER ISSUES OF NOC**	Periods	**9**
Energy and Power Issues in Networks-on-Chips-The CHAIN works Tool Suite: A Complete Industrial Design Flow for Networks-on-Chips			
Unit – IV	**MICRO-ARCHITECTURE OF NOC ROUTER**	Periods	**9**
Baseline NOC Architecture – MICRO-Architecture Exploration ViChaR: A Dynamic Virtual Channel Regulator for NOC Routers- ROCO: The Row-Column Decoupled Router – A Gracefully Degrading and Energy-Efficient Modular Router Architecture for On-Chip Networks. Exploring Fault Tolerant Networks-on-Chip Architectures			
Unit – V	**3D INTEGRATION OF NETWORK-ON-CHIP**	Periods	**9**
3D Networks-on-Chips Architectures–A Novel Dimensionally decomposed Router for On Chip Communication in 3D Architectures - Resource Allocation for QoS On-Chip Communication – Networks on-Chip Protocols-On chip Processor Traffic Modeling for Networks-on Chip.			
		Total Periods	**45**

References

1.	ChrysostomosNicopoulos, Vijaykrishnan Narayanan, Chita R.Da, "Networks-on – Chip Architectures a Holistic Design Exploration", Springer.2009.
2.	Santanu Kundu, Santanu Chattopadhyay, —Network-on-Chip: The Next Generation of System-on-Chip Integration‖, CRC press, 2014.
3.	Fayezgebali, Haythamelmiligi, HqhahedWatheq E1-Kharashi ,"Networks-on-Chips Theory and Practice," CRC Pres, 2009.
4.	Konstantinos Tatas and Kostas Siozios "Designing 2D and 3D Network-on-Chip Architectures" 2013.
5.	Palesi, Maurizio, Daneshtalab, Masoud "Routing Algorithms in Networks-on-Chip" 2014

E-Resources

E1	https://nptel.ac.in/courses/117105137/54CO-ORDINATED BY : IIT KHARAGPUR
E2	https://nptel.ac.in/courses/106103183/22CO-ORDINATED BY : IIT GUWAHATI

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Programme	**M.E.**	Programme Code	**205**	Regulation	**2023**
Department	**VLSI DESIGN / ELECTRONICS AND COMMUNICATION ENGINEERING**			Semester	--

Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P23VDE19	**ARM processor and architecture**	3	0	0	3	40	60	100

Course Objective

The main objective of the course is

- To apply the concepts of architecture and assembly language programming of ARM Processor.
- To compare the concepts of architectural support for high level language and memory hierarchy.
- To learn the software design and memory management.
- To study the concepts of architectural support for operating system
- To understand the concept of ARM Co-processor interface.

Course Outcome

At the end of the course, the student should be able to	Knowledge Level
CO1: Understand the different types of ARM architectures.	K4
CO2: Analyze about the assembly language program for various industry based applications	K4
CO3: Understand the concept of ARM Co-Processor Interface	K2
CO4: Describe the general architecture of ARM	K4
CO5: Understand the applications of ARM Processors.	K2

Pre-requisites

CO / PO Mapping
(3/2/1 indicates strength of correlation) 3-Strong, 2 – Medium, 1 - Weak

CO/PSO Mapping

Cos	Programme Outcomes (POs)												PSOs		
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2	PSO 3
CO 1	3	3	3	2									3		
CO 2	3	3	3	2									3		
CO 3	3	3	3	2									3	2	
CO 4	3	3	3	2										2	
CO 5	3	3	3	2										2	

Course Assessment Methods

Direct

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1. Continuous Assessment Test I, II & III
2. Assignment and Seminar
3. End-Semester examinations

Indirect

1. Course – end survey

Content of the syllabus

Unit – I	**ARM ARCHITECTURE**	Periods	**9**

Abstraction in hardware design – MU0 processor –Acorn RISC Machine – Architecture Inheritance – ARM programming model – ARM Development Tools – 3 and 5 Stage Pipeline ARM Organization – ARM Instruction Execution and Implementation – ARM Co-Processor Interface.

Unit – II	**ARM ASSEMBLY LANGUAGE PROGRAMMING**	Periods	**9**

ARM Instruction Types – Data transfer, Data Processing and Control Flow Instructions – Multiply instructions-swap instructions–Co-Processor Instructions: Data transfers, Register transfers.

Unit – III	**ARCHITECTURAL SUPPORT FOR HIGH LEVEL LANGUAGE AND MEMORY HIERARCHY**	Periods	**9**

Abstraction in software design – Data Types -expressions – Loops – Functions and Procedures – Conditional Statements – use of memory- Memory size and speed – On Chip Memory – Caches Design – an example – Memory management.

Unit – IV	**ARCHITECTURAL SUPPORT FOR SYSTEM DEVELOPMENT**	Periods	**9**

Advanced microcontroller bus Architecture(AMBA) – ARM memory Interface – ARM Reference Peripheral Specification– Hardware System Prototyping Tools – ARMulator – Debug Architecture

Unit – V	**ARCHITECTURAL SUPPORT FOR OPERATING SYSTEM**	Periods	**9**

An introduction to Operating systems – ARM system Control Coprocessor – CP15 Protection unit Registers –ARM Protection unit – CP15 MMU Registers – ARM MMU Architecture – Synchronization -context Switching- input and output. ARM applications: VLSI Ruby II Advanced Communication Processor.

	Total Periods	**45**

References

1.	Steve Furber, "ARM System on Chip Architecture", Addison –Wesley Professional, 2000
2.	Ricardo Reis, "Design of System on a Chip: Devices and Components", Springer, 2004
3.	Jason Andrews, "Verification of Hardware and Software for ARM System on Chip Design (EmbeddedTechnology)", Ewnes, BK and CD-ROM, Aug 2004.
4.	P.Rashinkar, L.Paterson and Singh, "System on a Chip Verification- Methodologies and Techniques", Kluwer Academic Publishers, 2000.

E-Resources

E1	https://nptel.ac.in/courses/117106111/CO-ORDINATED BY : IIT MADRAS
E2	https://nptel.ac.in/courses/108102045/5CO-ORDINATED BY : IIT DELHI

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	VIVEKANANDHACOLLEGEOFENGINEERINGFORWOMEN (AutonomousInstitution,AffiliatedtoAnnaUniversity,Chennai) Elayampalayam, Tiruchengode – 637 205						
Programme	M.E.	Programme Code	205	Regulation	2023		
Department	VLSI DESIGN/ELECTRONICSAND COMMUNICATION ENGINEERING			Semester	--		
Course Code	Course Name	Periods Per Week			Credit	Maximum Marks	
		L	T	P	C	CA	ESE	Total
P23VDE20	Wireless Adhoc and Sensor Networks	3	0	0	3	40	60	100

Course Objective

The main objective of the course is

- To understand the basics of Ad-hoc & Sensor Networks.
- To learn various fundamental and emerging protocols of all layers.
- To study about the issues pertaining to major obstacles in establishment and efficient management of Ad-hoc and sensor networks.
- To understand the nature and applications of Ad-hoc and sensor networks.
- TounderstandvarioussecuritypracticesandprotocolsofAd-hocandSensor Networks

Course Outcome

At the end of the course ,the student should be able to	Knowledge Level
CO1: Identify different issues in wireless Ad hoc and sensor networks.	K2
CO2: Analyze protocols developed for Ad hoc and sensor networks.	K4
CO3: Identify Multicast routing protocol in Ad hoc and sensor networks.	K2
CO4: Establish a Sensor network environment for different type of Applications.	K4
CO5: Understand various security practices and protocols of Ad-hoc wireless Networks	K2

Pre-requisites

CO / PO Mapping (3/2/1 indicates strength of correlation) 3-Strong, 2 – Medium, 1 - Weak													CO/PSO Mapping		
COs	Programme Outcomes (POs)												PSOs		
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PS O1	PSO 2	PS O 3
CO 1	3	2		1	1								2		
CO 2	3	3	2		1								2		
CO 3	3		2	1									2		
CO 4	3	2	2	1	1								2		
CO 5	3		1	1	1								2		

Course Assessment Methods

Direct

1. Continuous Assessment Test I,II&III
2. Assignment and Seminar
3. End-Semester examinations

Indirect

1. Course-end survey

Content of the syllabus

Unit –I	MAC&TCP IN AD HOC NETWORKS	Periods	9

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IEEE 802.3 Standard –IEEE 802.11 Standard - Self configuration and Auto configuration-Issues in Ad-Hoc Wireless Networks– Classification of MAC Protocols for Ad-Hoc Wireless Networks–Contention Based Protocols- TCP over Ad-Hoc networks-TCP protocol overview - TCP and MANETs – Solutions for TCP over Ad-Hoc Networks.			
Unit –II	**ROUTING IN AD HOC NETWORKS**	Periods	**9**
Introduction-Issues in design a Routing in Ad-Hoc Networks- Classification-Table driven –On demand-Hybrid – Routing Protocol with efficient flooding mechanisms-Hierarchical Routing Protocols-Power Aware Routing Protocols			
Unit –III	**MULTICAST ROUTING PROTOCOL IN ADHOC WIRELESS SENSOR NETWORKS**	Periods	**9**
Introduction – Issues in designing a Multicast Routing Protocol-Operation of Multicast routing protocol-Architecture – Classifications of multicast routing protocols-Tree based multicast routing protocols-Mutlicast Routing protocol based on Zone routing-Mutlicast core-Extraction Distributed Ad hoc Routing-Associativity-based Ad hoc Multicast routing.			
Unit –IV	**SENSOR MANAGEMENT**	Periods	**9**
Sensor Management-Topology Control Protocols and Sensing Mode Selection Protocols-Time synchronization-Localization and positioning–Operating systems and Sensor Network programming–Sensor Network Simulators.			
Unit –V	**SECURITY IN AD HOC WIRELESS NETWORKS**	Periods	**9**
Security in Ad-Hoc wireless networks–Network security requirements-Issues and challenges in security provisioning-Network security attacks-Key Management Approaches-Key Management in Ad hoc wireless networks–Secure routing in Ad hoc wireless networks			
		Total Periods	**45**

References

1.	AdrianPerrig,J.D.Tygar,—SecureBroadcastCommunication:InWiredandWireless Networks‖, Springer, 2006.
2.	CarlosDeMoraisCordeiro,DharmaPrakashAgrawal,—AdHocandSensorNetworks: Theory and Applications‖,2nd Edition, World Scientific Publishing,2011
3.	C.SivaRamMurthyandB.S.Manoj,—AdHocWirelessNetworks–Architecturesand Protocols‖, Pearson Education, 2004.
4.	C.K.Toh,—Ad Hoc Mobile Wireless Networks‖, PearsonEducation,2002.
5.	ErdalÇayırcı,ChunmingRong,—SecurityinWirelessAdHocandSensorNetworks‖,John WileyandSons,2009.
6.	HolgerKarl,Andreaswillig,—ProtocolsandArchitecturesforWirelessSensorNetworks‖, John Wiley & Sons, Inc .2005.
7.	Subir Kumar Sarkar,T G Basavaraju, C Puttamadappa,—Ad Hoc Mobile Wireless Networks‖,AuerbachPublications,2008.
8.	WaltenegusDargie,ChristianPoellabauer,—FundamentalsofWirelessSensor Networks Theory and Practice‖, John Wiley and Sons, 2010.

E-Resources

E1	https://nptel.ac.in/courses/106105160/21CO-ORDINATEDBY:IITKHARAGPUR
E2	https://nptel.ac.in/courses/106105160/CO-ORDINATEDBY:IITKHARAGPUR

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VIVEKANANDHA COLLEGE OF ENGINEERING FOR WOMEN
(Autonomous Institution, Affiliated to Anna University ,Chennai)
Elayampalayam, Tiruchengode – 637 205

Programme	**M.E.**	Programme Code	**205**	Regulation	**2023**
Department	**VLSI DESIGN / ELECTRONICS AND COMMUNICATION ENGINEERING**			Semester	**III**

Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P23VDOE1	**Micro sensors and MEMS**	3	0	0	3	40	60	100

Course Objective

The main objective of the course is

- To understand the micro fabrication process, MEMS materials and various system issues.
- To acquire basic knowledge on electrical and mechanical concepts of MEMS
- To acquire knowledge on various types of micro sensors.
- To introduce the concepts of optical and RF MEMS and various case studies
- To understand the concept of Optical MEMS

Course Outcome

At the end of the course, the student should be able to	Knowledge Level
CO1: Knowledge on micro fabrication process, MEMS materials and various system issues.	K3
CO2: Basic knowledge on electrical and mechanical concepts of MEMS	K2
CO3: Knowledge on various types of Micro sensors.	K3
CO4: Knowledge on optical and RF MEMS and various case studies.	K3
CO5: Basic knowledge on Active actuators for optical MEMS	K2

Pre-requisites

CO / PO Mapping (3/2/1 indicates strength of correlation) 3-Strong, 2 – Medium, 1 - Weak													**CO/PSO Mapping**		
Cos	Programme Outcomes (POs)												PSOs		
	PO 1	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO 10**	**PO 11**	**PO 12**	**PSO 1**	**PSO 2**	**PSO 3**
CO 1	3	2	2	2							2		3		
CO 2	3	2	2	2							2		3		
CO 3	3	2	2	2					2	2			3	2	
CO 4	3	2	2	2					2	2			3	2	
CO 5	3	2	2	2									3	2	

Course Assessment Methods

Direct

1. Continuous Assessment Test I, II & III
2. Assignment and Seminar
3. End-Semester examinations

Indirect

1. Course – end survey

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Content of the syllabus			
Unit – I	**MICROFABRICATION AND MATERIALS**	Periods	**9**
Introduction – Evolution of MEMS – Microsensors and actuators – Microfabrication – Lithography, Etching, Deposition, Oxidation, Diffusion – MEMS materials – Metals – Physical and chemical properties, Metallization – Semiconductors – Electrical and chemical properties, Growth and Deposition – Bulk and Surface micromachining.			
Unit – II	**ELECTRICAL AND MECHANICAL CONCEPTS**	Periods	**9**
Conductivity and resistivity – Elasticity – Stress and strain – Isotropic and Anisotropic materials – Bending of beams – types, Deflection – Pure bending – Torsional deflections – intrinsic stress – Resonance – Viscosity – Surface tension.			
Unit – III	**MEMS ISSUES AND CASE STUDIES**	Periods	**9**
Circuit and System issues – Electronics, Feedback systems and Noises. Case studies – Commercial pressure sensor, MEMS magnetic actuators, Capacitive accelerometer.			
Unit – IV	**TYPES OF MICROSENSORS**	Periods	**9**
Introduction – Thermal sensors, Radiation sensors, Mechanical sensors – Pressure microsensors and Flow microsensors, Magnetic sensors, Bio(Chemical) sensors – SAW-IDT microsensor – fabrication – applications – Strain, Temperature, Pressure and Humidity sensor.			
Unit – V	**OPTICAL AND RF MEMS**	Periods	**9**
Optical MEMS – Passive MEMS optical components – Lenses, Mirrors – Active actuators for optical MEMS – Translation and rotation motion – RF MEMS – Basics – Sample case studies of optical and RF MEMS.			
		Total Periods	**45**

References	
1.	StephenSanturia, "Microsystems Design", Kluwer publishers, 2000
2.	Julian w. Gardner, Vijay K. Varadan, Osama O. Awadelkarim, "Micro Sensors MEMS and Smart Devices", John Wiley & Son LTD, 2002.
3.	Chang Liu, "Foundations of MEMS", Pearson Education Inc., 2006.
4.	NadimMaluf, "An introduction to Micro electro mechanical system design", Artech House, 2000
E-Resources	
E1	www.sciencedirect.com
E2	https://iopscience.iop.org

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Programme	M.E.	Programme Code	205	Regulation	2023
Department	VLSI DESIGN / ELECTRONICS AND COMMUNICATION ENGINEERING			Semester	III

Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P23VDOE02	Basics of VLSI	3	0	0	3	40	60	100

Course Objective

The main objective of the course is

- To explain the operation and characteristics of MOS transistor
- To discuss the steps involved in fabrication of IC
- To discuss the concepts of circuit families for low power CMOS design
- To discuss the basic concepts of FPGA and ASIC
- Learn the concepts of modeling a digital system using Hardware Description Language and describe the current trends in VLSI

Course Outcome

At the end of the course, the student should be able to	Knowledge Level
CO1: Explain the operation and characteristics of MOS transistor	K2
CO2: List the steps involved in fabrication of IC and issues involved in fabrication	K4
CO3: Construct the low power CMOS VLSI Circuits	K3
CO4: Explain the different FPGA Architectures and Programmable Logic Devices	K2
CO5: Analyze the combinational and sequential circuits using Verilog HDL	K4

Pre-requisites -

CO / PO Mapping (3/2/1 indicates strength of correlation) 3-Strong, 2 – Medium, 1– Weak

CO/PSO Mapping

Cos	Programme Outcomes (Pos)												PSOs		
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2	PSO 3
CO 1	3	3	3	2					2				3		
CO 2	3	3	3	2					2	2			3	2	
CO 3	3	3	3	2				2		2			3	2	
CO 4	3	3	3	2				2					3	2	
CO 5	3	3	3	2										2	

Course Assessment Methods

Direct

1. Continuous Assessment Test I, II & III
2. Assignment and Seminar
3. End-Semester examinations

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Indirect
1. Course – end survey

Content of the syllabus

Unit – I	MOS DEVICES AND CIRCUITS	Periods	9
Evolution of Ics– Moore's law- VLSI design flow – MOS transistors - Ideal I-V and C-V characteristics, non-ideal I-V effects, DC transfer characteristics– Stick diagram and Layout diagram- Layout design rules- Realization of circuit using CMOS			
Unit – II	**FABRICATION OF CMOSs**	Periods	**9**
NMOS and CMOS fabrication – N-well, P-well and twin tub processes and SOI, Layout design Rules, CMOS Logic. Technology related CAD issues, manufacturing issues.			
Unit – III	**COMBINATIONAL CIRCUIT DESIGN**	Periods	**9**
Circuit Families- Static CMOS, Ratioed circuits, Cascode voltage switch logic, Dynamic circuits, Pass transistor circuits,BiCMOS, Realization of circuits using Circuit families			
Unit – IV	**IMPLEMENTATION STRATEGIES**	Periods	**9**
PLDs – PAL, PLA, CPLD, Full custom and Semi custom ASIC design- Standard cell design, FPGA building block architectures, FPGA interconnect – Routing – FPGA, Xilinx 4000 series –Altera Cyclone III			
Unit – V	**VERILOG HARDWARE DESCRIPTION LANGUAGE**	Periods	**9**
Introduction to Verilog HDL –Basic Concepts-Identifiers-Gate primitives, gate delays, operators, timing controls, procedural assignments, conditional assignments, Tasks and functions - Behavior modeling —Gate level modeling – Dataflow modeling- switch level modeling. Design examples - Combinational and sequential circuits using Verilog			
		Total Periods	**45**

References

1.	M.MorrisMano, Digital Design, 5th Edition, Prentice Hall of India Pvt.Ltd.,2003/ Pearson Education (Singapore) Pvt.Ltd., NewDelhi, 2018.
2.	Neil Weste& David Harris , "CMOS VLSI Design-A circuits & System Perspective", 4th Edition, Pearson education, New Delhi, 2017
3.	Palnitkar Samir, "Verilog HDL: Guide to Digital Design and synthesis", 2nd Edition, Pearson Education , New Delhi, 2017.
4.	Pucknell D.A and Eshraghian K , "Basic VLSI Design", PHI publication, Second Edition,2011
5.	Charles H. Roth, "Digital Systems Design Using VHDL", CL Engineering/CengageLearning India, 2012.
6.	M.J. Smith, "Application specific integrated circuits", Addison Wesley, 2008.
7.	JohnF.Wakerly, Digital Design,Fourth Edition,Pearson /PHI,2016

E-Resources

E1	www.electronicsforu.com
E2	www.vlsi-expert.com
E3	https://nptel.ac.in/courses/117106086/
E4	https://nptel.ac.in/content/syllabus_pdf/108105113.pdf

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Programme	**M.E.**	Programme Code		**205**	Regulation		**2023**	
Department	**VLSI DESIGN / ELECTRONICS AND COMMUNICATION ENGINEERING**				Semester		**III**	
Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P23VDOE3	**Communication Busses and Interfaces**	3	0	0	3	40	60	100

Course Objective

The main objective of the course is

- To Study the concepts of serial busses
- To Study the concepts of Low Speed Serial Bus Physical Interface
- To Understand the concepts of CAN
- To Understand the concepts of USB
- To Study the concepts of PCI

Course Outcome

At the end of the course, the student should be able to	Knowledge Level
CO1: Select Low speed Serial buses for various applications	K2
CO2: Demonstrate Low speed serial buses Configuration	K3
CO3: Interpret Automotive Bus Frame structure	K2
CO4: Analyze USB Descriptors	K4
CO5: Describe high speed PCIe bus configuration space	K2

Pre-requisites

CO / PO Mapping (3/2/1 indicates strength of correlation) 3-Strong, 2 – Medium, 1 - Weak													CO/PSO Mapping		
Cos	Programme Outcomes (POs)												PSOs		
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2	PSO 3
CO 1	3	3	3	2						2		2		2	
CO 2	3	3	3	2						2		2	3	2	
CO 3	3	3	3	2							2		3	2	
CO 4	3	3	3	2							2		3	2	
CO 5	3	3	3	2									3		

Course Assessment Methods

Direct

1. Continuous Assessment Test I, II & III
2. Assignment and Seminar
3. End-Semester examinations

Indirect

1. Course - end survey

Content of the syllabus

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Unit – I	**LOW SPEED SERIAL BUS ARCHITECTURE**	Periods	**9**
Serial Buses RS232, I2C, SPI Features, Frame structure, Control signals, Limitations.			
Unit – II	**LOW SPEED SERIAL BUS PHYSICAL INTERFACE**	Periods	**9**
Serial Buses RS232, RS485, I2C, SPI, Physical Interface, Configuration and applications			
Unit – III	**CAN ARCHITECTURE**	Periods	**9**
Features, Architecture, Frame structure, Physical Interface, Data transmission, Applications.			
Unit – IV	**USB ARCHITECTURE**	Periods	**9**
Transfer types, Enumeration, Descriptor types and contents, Device driver.			
Unit – V	**PCI ARCHITECTURE**	Periods	**9**
Revisions, Features, Configuration space, Hardware protocols, Applications.			
		Total Periods	**45**

References

1.	Axelson, J. Serial Port Complete: COM Ports, USB Virtual COM Ports, and Ports for Embedded Systems, ser, 2nd Edition, *Complete Guides Series. Lakeview Research* 2007.
2.	Axelson, Jan. *USB complete* . Lakeview Research, 2015.
3.	Mike Jackson, Ravi Budruk, "PCI Express Technology", Mindshare Press
4.	Wilfried Voss, *A Comprehensible Guide to Controller Area Network,* Copperhill Media Corporation, 2 nd Edition, 2005.
5.	Axelson, J. Serial Port Complete: COM Ports, USB Virtual COM Ports, and Ports for Embedded Systems, ser, 2nd Edition, *Complete Guides Series. Lakeview Research* 2007.
6.	Axelson, Jan. *USB complete* . Lakeview Research, 2015.

E-Resources

E1	Serial Front Panel Draft Standard VITA 17.1 – 200x
E2	Technical references on www.can-cia.org, www.pcisig.com, www.usb.org

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Programme	M.E	Programme Code	205	Regulation	2023
Department	VLSI DESIGN / ELECTRONICS AND COMMUNICATION ENGINEERING			Semester	

Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P23AC001	Research Process and Methodologies	2	0	0	0	100	-	100

Course Objective

The main objective of the course is

- To understand the importance of Research
- To acquire knowledge in Data Collection and Analysis
- To effectively write reports

Course Outcome

At the end of the course, the student should be able to	Knowledge Level
CO1: Understand research problem types and data collection methods.	K2
CO2: Understand research design methodologies	K2
CO3: Analyze research related information	K4
CO4: Follow research ethics	K2
CO5: Understand that today's world is controlled by Computer, Information Technology, but tomorrow world will be ruled by ideas, concept, and creativity.	K2

Pre-requisites --

CO / PO Mapping
(3/2/1 indicates strength of correlation) 3-Strong, 2 – Medium, 1 - Weak

CO/PSO Mapping

Cos	Programme Outcomes (POs)												PSOs		
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2	PSO 3
CO 1	3	3	3	2											
CO 2	3	3	3	2					2						
CO 3	3	3	3	2					2						
CO 4	3	3	3	2					2						
CO 5	3	3	3	2											

Course Assessment Methods

Direct
1. Continuous Assessment Test I, II & III
2. Assignment and Seminar
Indirect
1. Course - end survey

Content of the syllabus

Unit - I	INTRODUCTION TO RESEARCH	Periods	9

Meaning of research problem, Sources of research problem, Criteria Characteristics of a good research Meaning of Research - Types of Research - Research Process - Problem definition - Objectives of Research - Research design - Approaches to Research - Quantitative vs. Qualitative Approach - Research Methods versus Methodology - Research and Scientific Method - Research Process - Criteria of Good Research.

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Unit – II	RESEARCH DESIGN	Periods	9
Meaning of Research Design - Need for Research Design - Features of a Good Design - Important Concepts Relating to Research Design - Different Research Designs - Basic Principles of Experimental Designs.			
Unit – III	**DATA COLLECTION**	Periods	**9**
Data Collection: Collection of Primary Data - Observation Method - Interview Method - Collection of Data through Questionnaires - Collection of Data through Schedules - Difference between Questionnaires and Schedules - Collection of Secondary Data - Processing Operations - Elements/Types of Analysis - Statistics in Research.			
Unit – IV	**DATA ANALYSIS AND INTERPRETATION**	Periods	**9**
Data analysis - Statistical techniques and choosing an appropriate statistical technique - Hypothesis, Hypothesis testing - Data processing software (e.g. SPSS etc.) - statistical inference - Interpretation of results.			
Unit - V	**REPORT WRITING**	Periods	**9**
Types of research report: Dissertation and Thesis, research paper, review article, short communication, conference presentation etc., Referencing and referencing styles, Research Journals, Indexing and citation of Journals, Intellectual property, Plagiarism.			
		Total Periods	**45**

References

1.	C. R. Kothari, "Research Methodology – Methods and Techniques", 2nd Edition, New Age International Publishers
2.	Bordens, K. S. and Abbott, B. B., "Research Design and Methods – A Process Approach", 8th Edition, McGraw-Hill, 2011
3.	Robert P. Merges, Peter S. Menell, Mark A. Lemley, "Intellectual Property in New Technological Age", 2016.
4.	Davis, M., Davis K., and Dunagan M., "Scientific Papers and Presentations", 3rd Edition, Elsevier Inc.

E-Resources

1.	https://www.oreilly.com/library/view/research-methodology/9789353067090/
2.	https://bbamantra.com/research-methodology/

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Programme	M.E	Programme Code	205	Regulation	2023
Department	VLSI DESIGN / ELECTRONICS AND COMMUNICATION ENGINEERING		Semester		

Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P23AC002	Pedagogy Studies	2	0	0	0	100	-	100

Course Objective

The main objective of the course is

- Understand the concept of programme design through evidences.
- Illustrate the practice of innovative teaching methodology.
- Analyze the method of teacher education.
- Enhance the infrastructure in the class room.
- Elaborate the directions of future research

Course Outcome	At the end of the course, the student should be able to	Knowledge Level
	CO1: Describe about the concept of programme design through evidences	K2
	CO2: Demonstrate the practice of innovative teaching methodology	K2
	CO3: Evaluate the method of teacher education	K4
	CO4: Examine the infrastructure in the class room	K3
	CO5: Define the directions of future research	K3

Pre-requisites -

CO / PO Mapping (3/2/1 indicates strength of correlation) 3-Strong, 2 – Medium, 1 - Weak													CO/PSO Mapping		
Cos	Programme Outcomes (POs)												PSOs		
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2	PSO 3
CO 1	3	3	3	2											
CO 2	3	3	3	2											
CO 3	3	3	3	2						2	2				
CO 4	3	3	2	2						2	2				
CO 5	3	3	2	2											

Course Assessment Methods

Direct
1. Continuous Assessment Test I, II & III 2. Assignment and Seminar
Indirect
1. Course - end survey

Content of the syllabus

Unit - I	INTRODUCTION	Periods	9

Introduction and Methodology: Aims and rationale, Policy background, Conceptual framework and terminology, Theories of learning, Curriculum, Teacher education. Conceptual framework, Research questions. Overview of methodology and Searching.

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Unit – II	THEMATIC OVERVIEW	Periods	9
Thematic overview: Pedagogical practices are being used by teachers in formal and informal classrooms in developing countries. Curriculum, Teacher education.			
Unit – III	**PEDAGOGICAL PRACTICES**	Periods	**9**
Evidence on the effectiveness of pedagogical practices Methodology for the in depth stage: quality assessment of included studies. How can teacher education (curriculum and practicum) and the school curriculum and guidance materials best support effective pedagogy? Theory of change. Strength and nature of the body of evidence for effective pedagogical practices. Pedagogic theory and pedagogical approaches. Teachers' attitudes and beliefs and Pedagogic strategies.			
Unit – IV	**PROFESSIONAL DEVELOPMENT**	Periods	**9**
Professional development: alignment with classroom practices and follow-up support -Peer support from the head teacher and the community. Curriculum and assessment Barriers to learning: limited resources and large class sizes.			
Unit - V	**RESEARCH GAPS AND FUTURE DIRECTIONS**	Periods	**9**
Research gaps and future directions, Research design, Contexts, Pedagogy, Teacher education, Curriculum and assessment, Dissemination and research impact.			
		Total Periods	**45**

References

1.	Ackers J, Hardman F (2001) Classroom interaction in Kenyan primary schools, Compare, 31 (2): 245-261.
2.	Agrawal M (2004) Curricular reform in schools: The importance of evaluation, Journal of Curriculum Studies, 36 (3): 361-379.
3.	Akyeampong K (2003) Teacher training in Ghana - does it count? Multi-site teacher education research project (MUSTER) country report 1. London: DFID.

E-Resources

1.	https://nptel.ac.in/courses/121/105/121105010/ CO-ORDINATED BY : IIT KHARAGPUR
2.	https://nptel.ac.in/courses/109/105/109105122/ CO-ORDINATED BY : IIT KHARAGPUR

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Programme	M.E	Programme Code	205	Regulation	2023
Department	VLSI DESIGN / ELECTRONICS AND COMMUNICATION ENGINEERING			Semester	

Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P23AC003	Disaster Management	2	0	0	0	100	-	100

Course Objective

The main objective of the course is

- Learn to demonstrate a critical understanding of key concepts in disaster risk reduction and humanitarian response.
- Critically evaluate disaster risk reduction and humanitarian response policy and practice from multiple perspectives.
- Develop an understanding of standards of humanitarian response and practical relevance in specific types of disasters and conflict situations.
- Critically understand the strengths and weaknesses of disaster management approaches, planning and programming in different countries, particularly their home country or the countries they work.
- Categorize the Risk Assessment in national level and global level.

Course Outcome

At the end of the course, the student should be able to	Knowledge Level
CO1: Understand the effects of disaster	K2
CO2: Analyze differences between disasters and hazards	K2
CO3: Disaster management techniques	K3
CO4: Risk management techniques	K3
CO5: Elaborate the Risk assessment in world level	K4

Pre-requisites --

CO / PO Mapping (3/2/1 indicates strength of correlation) 3-Strong, 2 – Medium, 1 - Weak													CO/PSO Mapping		
Cos	Programme Outcomes (POs)												PSOs		
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2	PSO 3
CO 1					2	2	2				2	1			
CO 2					2	2	2				2	1			
CO 3					2	2	2				2	1			
CO 4					2	2	2				2	1			
CO 5					2	2	2				2	1			

Course Assessment Methods

Direct
1. Continuous Assessment Test I, II & III
2. Assignment and Seminar
Indirect
1. Course - end survey

Content of the syllabus

Unit - I	INTRODUCTION	Periods	9

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Introduction Disaster: Definition, Factors and Significance; Difference Between Hazard and Disaster; Natural and Manmade Disasters: Difference, Nature, Types and Magnitude.			
Unit – II	**REPERCUSSIONS OF DISASTERS AND HAZARDS**	Periods	**9**
Repercussions of Disasters and Hazards: Economic Damage, Loss of Human and Animal Life, Destruction of Ecosystem. Natural Disasters: Earthquakes, Volcanisms, Cyclones, Tsunamis, Floods, Droughts and Famines, Landslides and Avalanches, Man-made disaster: Nuclear Reactor Meltdown, Industrial Accidents, Oil Slicks and Spills, Outbreaks of Disease and Epidemics, War and Conflicts.			
Unit – III	**DISASTER PRONE AREAS IN INDIA**	Periods	**9**
Disaster Prone Areas in India Study of Seismic Zones; Areas Prone to Floods and Droughts, Landslides and Avalanches; Areas Prone to Cyclonic and Coastal Hazards with Special Reference to Tsunami; Post-Disaster Diseases and Epidemics			
Unit – IV	**DISASTER PREPAREDNESS AND MANAGEMENT PREPAREDNESS**	Periods	**9**
Disaster Preparedness and Management Preparedness: Monitoring of Phenomena Triggering A Disaster or Hazard; Evaluation of Risk: Application of Remote Sensing, Data from Meteorological and Other Agencies, Media Reports: Governmental and Community Preparedness.			
Unit – IV	**RISK ASSESSMENT**	Periods	**9**
Risk Assessment Disaster Risk: Concept and Elements, Disaster Risk Reduction, Global and National Disaster Risk Situation. Techniques of Risk Assessment, Global Co-Operation in Risk Assessment and Warning, People's Participation in Risk Assessment. Strategies for Survival. Disaster Mitigation Meaning, Concept and Strategies of Disaster Mitigation, Emerging Trends in Mitigation. Structural Mitigation and Non-Structural Mitigation, Programs of Disaster Mitigation in India.			
		Total Periods	**45**
References			
1.	R. Nishith, Singh AK, "Disaster Management in India: Perspectives, issues and strategies "'New Royal book Company.		
2.	Sahni, Pardeep et.al. (Eds.)," Disaster Mitigation Experiences and Reflections", Prentice Hall of India, New Delhi.		
3.	Goel S. L., Disaster Administration and Management Text And Case Studies", Deep & Deep Publication Pvt. Ltd., New Delhi.		
E-Resources			
1.	https://www.digimat.in/nptel/courses/video/124107010/L36.html		
2.	https://media.ifrc.org/ifrc/what-we-do/disaster-and-crisis-management/disaster-preparedness/		

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Programme	M.E	Programme Code	205	Regulation	2023
Department	VLSI DESIGN / ELECTRONICS AND COMMUNICATION ENGINEERING			Semester	

Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P23AC004	Value Education	2	0	0	0	100	-	100

Course Objective

The main objective of the course is

- To introduce the value of education and self- development.
- To interpret good values in students.
- To elaborate the importance of character.
- To distinguish the relationship and their cooperation.
- To interpret the religions and equality.

Course Outcome

At the end of the course, the student should be able to	Knowledge Level
CO1: Understand education values	K2
CO2: Analyze importance of cultivation values	K2
CO3: Importance of personality development	K3
CO4: Character maintenance	K3
CO5: Examine the religions and honesty.	K4

Pre-requisites -

CO / PO Mapping
(3/2/1 indicates strength of correlation) 3-Strong, 2 – Medium, 1 - Weak

CO/PSO Mapping

Cos	Programme Outcomes (POs)												PSOs		
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2	PSO 3
CO 1	3	3	3	2											
CO 2	3	3	3	2											
CO 3	3	3	3	2											
CO 4	3	3	3	2											
CO 5	3	3	3	2											

Course Assessment Methods

Direct
1. Continuous Assessment Test I, II & III
2. Assignment and Seminar

Indirect
1. Course - end survey

Content of the syllabus

Unit - I	INTRODUCTION	Periods	9

Values and self-development –Social values and individual attitudes. Work ethics, Indian vision of humanism. Moral and non- moral valuation, Standards and principles, Value judgments.

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Unit – II	IMPORTANCE OF CULTIVATION OF VALUES	Periods	9
Importance of cultivation of values. Sense of duty. Devotion, Self-reliance. Confidence, Concentration. Truthfulness, Cleanliness. Honesty, Humanity. Power of faith, National Unity. Patriotism. Love for nature, Discipline.			
Unit – III	**PERSONALITY AND BEHAVIOR DEVELOPMENT**	Periods	**9**
Personality and Behavior Development - Soul and Scientific attitude. Positive Thinking. Integrity and discipline. Punctuality, Love and Kindness. Avoid fault Thinking. Free from anger, Dignity of labour.			
Unit – IV	**RELATIONSHIP MANAGEMENT**	Periods	**9**
Universal brotherhood and religious tolerance True friendship. Happiness Vs suffering, love for truth. Aware of self-destructive habits. Association and Cooperation. Doing best for saving nature.			
Unit - V	**CHARACTER AND COMPETENCE**	Periods	**9**
Character and Competence –Holy books vs Blind faith. Self-management and Good health. Science of reincarnation. Equality, Nonviolence, Humility, Role of Women. All religions and same message. Mind your Mind, Self-control. Honesty, Studying effectively.			
		Total Periods	**45**

References	
1.	Chakroborty, S.K. "Values and Ethics for organizations Theory and practice", Oxford University Press, New Delhi 2011.
E-Resources	
1.	https://www.ncbi.nlm.nih.gov/pmc/articles/PMC5132380/
2.	https://www.examrace.com/Study-Material/Education/Value-Education-YouTube-Lecture-Handouts.html

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Programme	M.E	Programme Code	205	Regulation	2023
Department	VLSI DESIGN / ELECTRONICS AND COMMUNICATION ENGINEERING			Semester	

Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P23AC005	Constitution of India	2	0	0	0	100	-	100

Course Objective

The main objective of the course is

- To understand the premises informing the twin themes of liberty and freedom from a civil rights perspective.
- To identify the growth of Indian opinion regarding modern Indian intellectuals' constitutional role and entitlement to civil and economic rights as well as the emergence of nationhood in the early years of Indian nationalism.
- To illustrate the role of socialism in India after the commencement of the Bolshevik Revolution and its impact on the initial drafting of the Indian Constitution.
- To categorize the governance bodies in the organization.
- To interpret the various administration in states.

Course Outcome

At the end of the course, the student should be able to	Knowledge Level
CO1: Define the history of Indian Constitution	K2
CO2: Categorize the importance of constitutional rights and duties.	K3
CO3:Understand the functions of Local administration	K2
CO4: Demonstrate the governance bodies in the organization.	K4
CO5: Prioritize the local and district administration in states.	K4

Pre-requisites --

CO / PO Mapping
(3/2/1 indicates strength of correlation) 3-Strong, 2 – Medium, 1 - Weak

CO/PSO Mapping

Cos	Programme Outcomes (POs)												PSOs		
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2	PSO 3
CO 1	3	3	2	2											
CO 2	3	3	2	2											
CO 3	3	3	2	2											
CO 4	3	3	2	2											
CO 5	3	3	2	2											

Course Assessment Methods

Direct

1. Continuous Assessment Test I, II & III
2. Assignment and Seminar

Indirect

1. Course - end survey

Content of the syllabus

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Unit - I	INTRODUCTION	Periods	9
History of Making of the Indian Constitution: History Drafting Committee, (Composition & Working)			
Unit – II	**PHILOSOPHY OF THE INDIAN CONSTITUTION**	Periods	**9**
Philosophy of the Indian Constitution: Preamble, Salient Features			
Unit – III	**CONTOURS OF CONSTITUTIONAL RIGHTS & DUTIES**	Periods	**9**
Contours of Constitutional Rights& Duties: Fundamental Rights- Right to Equality- Right to Freedom Right against Exploitation- Right to Freedom of Religion ,Cultural and Educational Rights, Right to Constitutional Remedies, Directive Principles of State Policy, Fundamental Duties			
Unit – IV	**ORGANS OF GOVERNANCE**	Periods	**9**
Organs of Governance: Parliament, Composition, Qualifications and Disqualifications, Powers and Functions, Executive, President, Governor, Council of Ministers, Judiciary, Appointment and Transfer of Judges, Qualifications, Powers and Functions.			
Unit - V	**LOCAL ADMINISTRATION**	Periods	**9**
Local Administration: District's Administration head: Role and Importance, Municipalities: Introduction, Mayor and role of Elected Representative, CEO of Municipal Corporation. Pachayati raj: Introduction, PRI: ZilaPachayat. Elected officials and their roles, CEO ZilaPachayat: Position and role. Block level: Organizational Hierarchy (Different departments) Village level: Role of Elected and Appointed officials, Importance of grass root democracy			
		Total Periods	**45**

References	
1.	The Constitution of India, 1950 (Bare Act), Government Publication.
2.	Dr. S. N. Busi, Dr. B. R. Ambedkar framing of Indian Constitution, 1st Edition, 2015.
3.	M. P. Jain, Indian Constitution Law, 7th Edition., Lexis Nexis, 2014.
E-Resources	
1.	https://nptel.ac.in/courses/129/106/129106002/ CO-ORDINATED BY : IIT MADRAS
2.	https://niti.gov.in/niti-lecture

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Programme	**M.E**	Programme Code		**205**	Regulation		**2023**
Department	**VLSI DESIGN / ELECTRONICS AND COMMUNICATION ENGINEERING**				Semester		
Course Code	Course Name	Periods Per Week			Credit	Maximum Marks	
		L	T	P	C	CA	ESE	Total
P23AC006	**English for Research Paper Writing**	2	0	0	0	100	-	100

Course Objective

The main objective of the course is

- Illustrate the improve your writing skills and level of readability
- Categorize to write in each section.
- Understand the skills needed when writing a Title
- Ensure the good quality of paper at very first-time submission.
- Elaborate the concept of writing skills for submission of paper.

Course Outcome

At the end of the course, the student should be able to	Knowledge Level
CO1: Understand forming and brake up sentences.	K2
CO2: Importance of finding plagiarism.	K4
CO3: Summarize the concept of literature reviews.	K2
CO4: Extend the focus on skill development activities.	K2
CO5: Develop the writing skills in the paper.	K3

Pre-requisites --

CO / PO Mapping (3/2/1 indicates strength of correlation) 3-Strong, 2 – Medium, 1 - Weak													CO/PSO Mapping		
Cos	Programme Outcomes (POs)												PSOs		
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2	PSO 3
CO 1	3	3	3	2											
CO 2	3	3	3	2											
CO 3	3	3	3	2											
CO 4	3	3	3	2											
CO 5	3	3	2	2											

Course Assessment Methods

Direct
1. Continuous Assessment Test I, II & III 2. Assignment and Seminar
Indirect
1. Course - end survey

Content of the syllabus

Unit - I	PLANNING AND PREPARATION	Periods	9

Planning and Preparation, Word Order, Breaking up long sentences, Structuring Paragraphs and Sentences, Being Concise and Removing Redundancy, Avoiding Ambiguity and Vagueness.

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Unit – II	CLARIFICATIONS	Periods	9
Clarifying Who Did What, Highlighting Your Findings, Hedging and Criticising, Paraphrasing and Plagiarism, Sections of a Paper, Abstracts. Introduction.			
Unit – III	**LITERATURE REVIEW**	Periods	9
Review of the Literature, Methods, Results, Discussion, Conclusions, The Final Check.			
Unit – IV	**SKILL DEVELOPMENT - I**	Periods	9
Key skills are needed when writing a Title, key skills are needed when writing an Abstract, key skills are needed when writing an Introduction, skills needed when writing a Review of the Literature.			
Unit - V	**SKILL DEVELOPMENT - II**	Periods	9
Skills are needed when writing the Methods, skills needed when writing the Results, skills are needed when writing the Discussion, skills are needed when writing the Conclusions, useful phrases, how to ensure paper is as good as it could possibly be the first- time submission			
		Total Periods	**45**

References	
1.	Goldbort R (2006) Writing for Science, Yale University Press (available on Google Books)
2.	Day R (2006) How to Write and Publish a Scientific Paper, Cambridge University Press
3.	Adrian Wallwork, English for Writing Research Papers, Springer New York Dordrecht Heidelberg London, 2011
E-Resources	
1.	https://nptel.ac.in/courses/110/105/110105091/ CO-ORDINATED BY : IIT KHARAGPUR
2.	https://www.udemy.com/topic/research-paper-writing

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Programme	M.E	Programme Code		205	Regulation	2023	
Department	VLSI DESIGN / ELECTRONICS AND COMMUNICATION ENGINEERING			Semester			

Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P23AC007	Personality Development through Life Enlightenment Skills	2	0	0	0	100	-	100

Course Objective

The main objective of the course is

- Learn to achieve the highest goal happily.
- Identify a person with stable mind, pleasing personality and determination.
- Determine wisdom in students.
- Interpret managing others effectively.
- Extend the increasing productivity.

Course Outcome	At the end of the course, the student should be able to	Knowledge Level
	CO1: Identify goals	K2
	CO2: Analyze Personality development	K2
	CO3: Make use of appropriate life and career goals	K3
	CO4: Developing relationships with others	K3
	CO5: Understand the value of diversity	K2

Pre-requisites --

CO / PO Mapping (3/2/1 indicates strength of correlation) 3-Strong, 2 – Medium, 1 - Weak — **CO/PSO Mapping**

Cos	Programme Outcomes (POs)												PSOs		
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2	PSO 3
CO 1	3	3	3	2					2						
CO 2	3	3	3	2					2						
CO 3	3	3	3	2					2	2					
CO 4	3	3	3	2						2					
CO 5	3	3	3	2											

Course Assessment Methods

Direct

1. Continuous Assessment Test I, II & III
2. Assignment and Seminar

Indirect

1. Course - end survey

Content of the syllabus

Unit - I	NEETISATAKAM – I	Periods	9

Neetisatakam-Holistic development of personality
Verses- 19,20,21,22 (wisdom)
Verses- 29,31,32 (pride & heroism)
Verses- 26,28,63,65 (virtue)

Unit – II	NEETISATAKAM – II	Periods	9

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Neetisatakam-Holistic development of personality Verses- 52,53,59 (dont's) Verses- 71,73,75,78 (do's)			
Unit – III	**APPROACH TO DAY TO DAY WORK AND DUTIES**	Periods	**9**
Approach to day to day work and duties. Shrimad Bhagwad Geeta : Chapter 2-Verses 41, 47,48, Chapter 3-Verses 13, 21, 27, 35, Chapter 6-Verses 5,13,17, 23, 35, Chapter 18-Verses 45, 46, 48.			
Unit – IV	**STATEMENTS OF BASIC KNOWLEDGE**	Periods	**9**
Statements of basic knowledge. Shrimad Bhagwad Geeta: Chapter2-Verses 56, 62, 68 Chapter 12 -Verses 13, 14, 15, 16,17, 18			
Unit - V	**PERSONALITY OF ROLE MODEL**	Periods	**9**
Personality of Role model. Shrimad Bhagwad Geeta: Chapter2-Verses 17, Chapter 3-Verses 36,37,42, Chapter 4-Verses 18, 38,39 Chapter18 – Verses 37,38,63			
		Total Periods	**45**
References			
1.	"Srimad Bhagavad Gita" by Swami SwarupanandaAdvaita Ashram (Publication Department), Kolkata		
2.	Bhartrihari's Three Satakam (Niti-sringar-vairagya) by P.Gopinath,		
3.	Rashtriya Sanskrit Sansthanam, New Delhi.		
E-Resources			
1.	https://library.um.edu.mo/ebooks/b17771201.pdf		
2.	https://www.staticcontents.youth4work.com/university/Documents/Colleges/CollegeSummaryAttach/29f57018-6412-4dee-b24b-ac29e54a0f9e.pdf		

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Programme	M.E	Programme Code	205	Regulation	2023
Department	VLSI DESIGN / ELECTRONICS AND COMMUNICATION ENGINEERING		Semester		

Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P23AC008	UNIVERSAL HUMAN VALUES	2	0	0	0	100	-	100

Course Objective

The student should be made to,

- To assist students in understanding the differences between values and skills, and in understanding the need, basic guidelines, content and the process of value education.
- To help students initiate a process of dialog within themselves to understand what they 'really want to be' in their lives and professions
- To help students understand the meaning of happiness and prosperity for human beings.
- To help students understand harmony at all the levels of human living and to lead an ethical life

Course Outcome

At the end of the course, the student should be able to	Knowledge Level
At the end of the course, the student should be able to,	K2
CO1: Evaluate the significance of value inputs in formal education and start applying them in their life and profession	K4
CO2: Distinguish between values and skills, happiness and accumulation of physical facilities, the Self and the Body, Intention and Competence of an individual, etc.	K2
CO3: Analyze the value of harmonious relationship based on trust and respect in their life and profession	K2
CO4: Examine the role of a human being in ensuring harmony in society and nature.	K3

Pre-requisites --

CO / PO Mapping
(3/2/1 indicates strength of correlation) 3-Strong, 2 – Medium, 1 - Weak

CO/PSO Mapping

COs	Programme Outcomes (POs)												PSOs		
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2	PSO 3
CO 1	1	1		3	3	1	2	3	3	2	3	1			
CO 2	2	1	2	3	2	2	2	2	1	1	3	1			
CO 3	3	1	2	3	3	1	3	2	2	1	2	3			
CO4	1	2	3	1	3	2	2	2	3	1	2	1			
CO5	2	1	2	1	2	1	3	3	2	2	1				

Course Assessment Methods

Direct

1. Continuous Assessment Test I, II & III
2. Assignment and Seminar

Indirect

1. Course - end survey

Content of the syllabus

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Unit - I	Introduction-Basic Human Aspiration	Periods	9
The basic human aspirations and their fulfillment through Right understanding and Resolution, Right understanding and Resolution as the activities of the Self, Self being central to Human Existence; All-encompassing Resolution for a Human Being, its details and solution of problems in the light of Resolution.			
Unit – II	**Right Understanding (Knowing)**	Periods	**9**
The domain of right understanding starting from understanding the human being (the knower, the experiencer and the doer) and extending up to understanding nature/existence – its interconnectedness and co-existence; and finally understanding the role of human being in existence (human conduct).			
Unit – III	**Understanding Human Being**	Periods	**9**
Understanding the human being comprehensively as the first step and the core theme of this course; human being as co-existence of the self and the body; the activities and potentialities of the self; Basis for harmony/contradiction in the self			
Unit – IV	**Understanding Nature and Existence**	Periods	**9**
A comprehensive understanding (knowledge) about the existence, Nature being included; the need and process of inner evolution (through self-exploration, self awareness and self-evaluation), particularly awakening to activities of the Self: Realization, Understanding and Contemplation in the self.			
Unit - V	**Understanding Human Conduct**	Periods	**9**
Understanding Human Conduct, different aspects of All-encompassing Resolution (understanding, wisdom, science etc.), Holistic way of living for Human Being with Allen compassing Resolution covering all four dimensions of human endeavor viz., realization, thought, behavior and work (participation in the larger order) leading to harmony at all levels from Self to Nature and entire Existence			
		Total Periods	**45**

Text Books	
1.	R R Gaur, R Asthana, G P Bagaria, 2019 (2nd Revised Edition), A Foundation Course in Human Values and Professional Ethics. ISBN 978-93-87034-47-1, Excel Books, New Delhi.
2.	Premvir Kapoor, Professional Ethics and Human Values, Khanna Book Publishing, New Delhi, 2022.
References E-Resources	
1.	Ivan Illich, 1974, Energy & Equity, The Trinity Press, Worcester, and Harper Collins, USA
2.	E.F. Schumacher, 1973, Small is Beautiful: a study of economics as if people mattered, Blond & Briggs, Britain
E-Resources	
1.	https://nptel.ac.in/courses/109104068
2.	https://fdp-si.aicte-india.org/UHV-I

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Programme	M.E	Programme Code			205	Regulation		2023
Department	VLSI DESIGN / ELECTRONICS AND COMMUNICATION ENGINEERING					Semester		
Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P23AC009	Online Course	2	0	0	0	100	-	100

Course Objective	The main objective of the course is • Illustrate about various online certification courses. • Understand the importance of online certification courses. • Distinguish about job opportunities. • Make use of this course can prepare the competitive examination. • Classify the online tools for course.

Course Outcome	At the end of the course, the student should be able to	Knowledge Level
	CO1: Evaluate the programming skills.	K3
	CO2: Identify online certifications.	K2
	CO3: Appraise the value of the courses and job opportunities	K5
	CO4: Categorize in Quantitative Reasoning and Technological Literacy.	K4
	CO5: Develop the ICT tools for the specific course.	K4
Pre-requisites	--	

CO / PO Mapping (3/2/1 indicates strength of correlation) 3-Strong, 2 – Medium, 1 - Weak													CO/PSO Mapping		
Cos	Programme Outcomes (POs)												PSOs		
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2	PSO 3
CO 1	3	3	2	2						2					
CO 2	3	3	2	2						2					
CO 3	3	3	2	2						2	2				
CO 4	3	3	2	2						2	2				
CO 5	3	3	2	2							2				

Course Assessment Methods

Direct
1. Online Assignments and Assessments
Indirect
1. Course - end survey

LIST OF COURSES

Online Courses such as :

1. NPTEL Courses
2. SWAYAM Courses
3. IIT-B Spoken Tutorials
4. UDEMY Courses
5. CCNA Courses
6. MOOC Courses
7. Microsoft Virtual Academy Certification courses etc.,

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